EC800M-CN

Reference Design

LTE Standard Module Series

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About the Document

Revision History

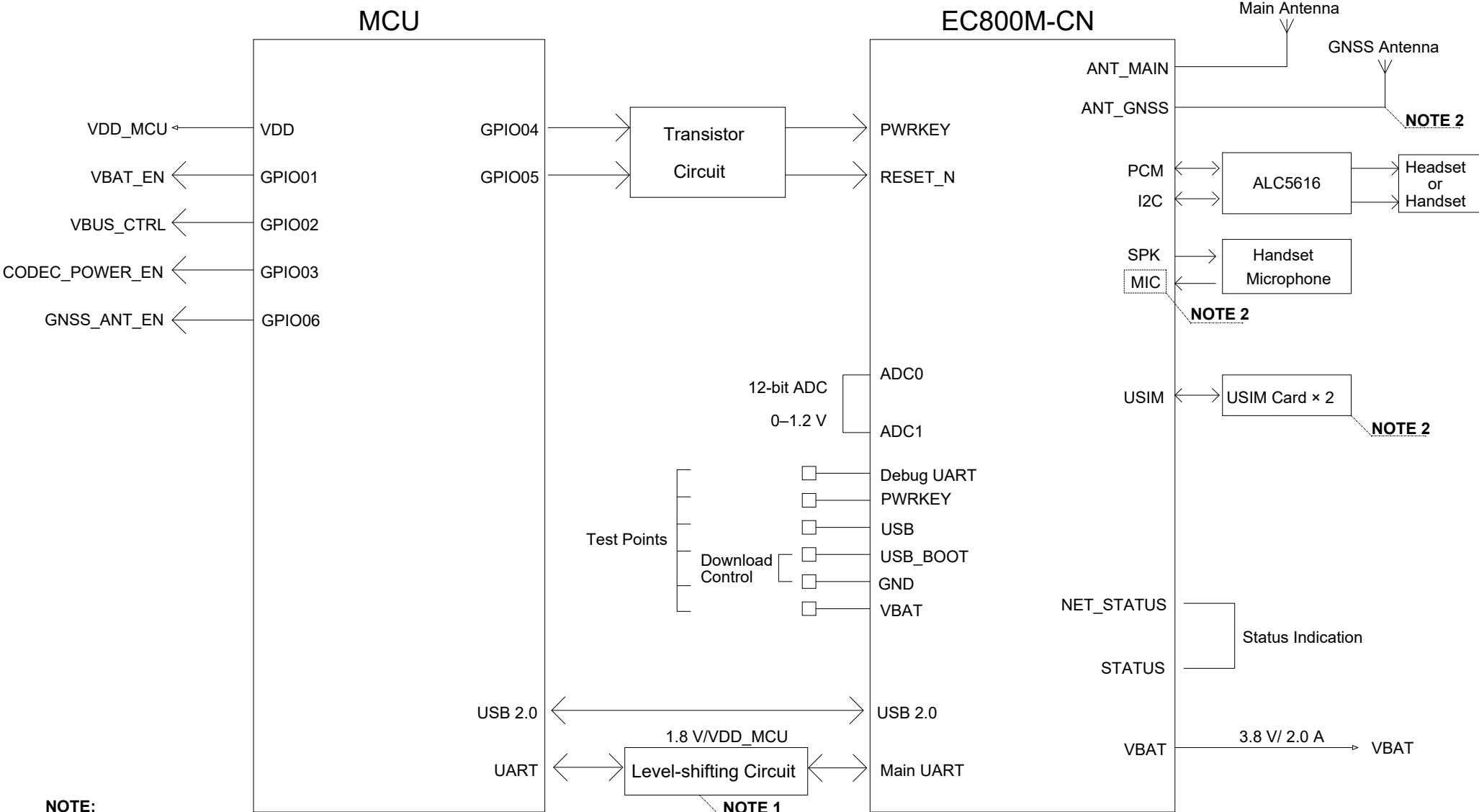| Version	Date	Author	Description
-	2022-05-26	Kelly WANG	Creation of the document
1.0	2022-09-20	Kelly WANG	First official release

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EC800M-CN module.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram

MCU

- VDD_MCU → VDD
- VBAT_EN ← GPIO01
- VBUS_CTRL ← GPIO02
- CODEC_POWER_EN ← GPIO03
- GNSS_ANT_EN ← GPIO06

- GPIO04 → Transistor Circuit
- GPIO05 → Transistor Circuit

- 12-bit ADC
- 0–1.2 V

Test Points
Download Control

- USB 2.0
- UART

EC800M-CN

- ANT_MAIN → Main Antenna
- ANT_GNSS → GNSS Antenna — **NOTE 2**

- Transistor Circuit → PWRKEY
- Transistor Circuit → RESET_N

- PCM ↔ ALC5616
- I2C ↔ ALC5616
- ALC5616 → Headset or Handset

- SPK → Handset Microphone
- MIC ← Handset Microphone — **NOTE 2**

- ADC0
- ADC1

- USIM ↔ USIM Card × 2 — **NOTE 2**

- Debug UART
- PWRKEY
- USB
- USB_BOOT
- GND
- VBAT

- NET_STATUS → Status Indication
- STATUS → Status Indication

- USB 2.0 ↔ USB 2.0
- 1.8 V/VDD_MCU → Level-shifting Circuit ↔ Main UART — **NOTE 1**
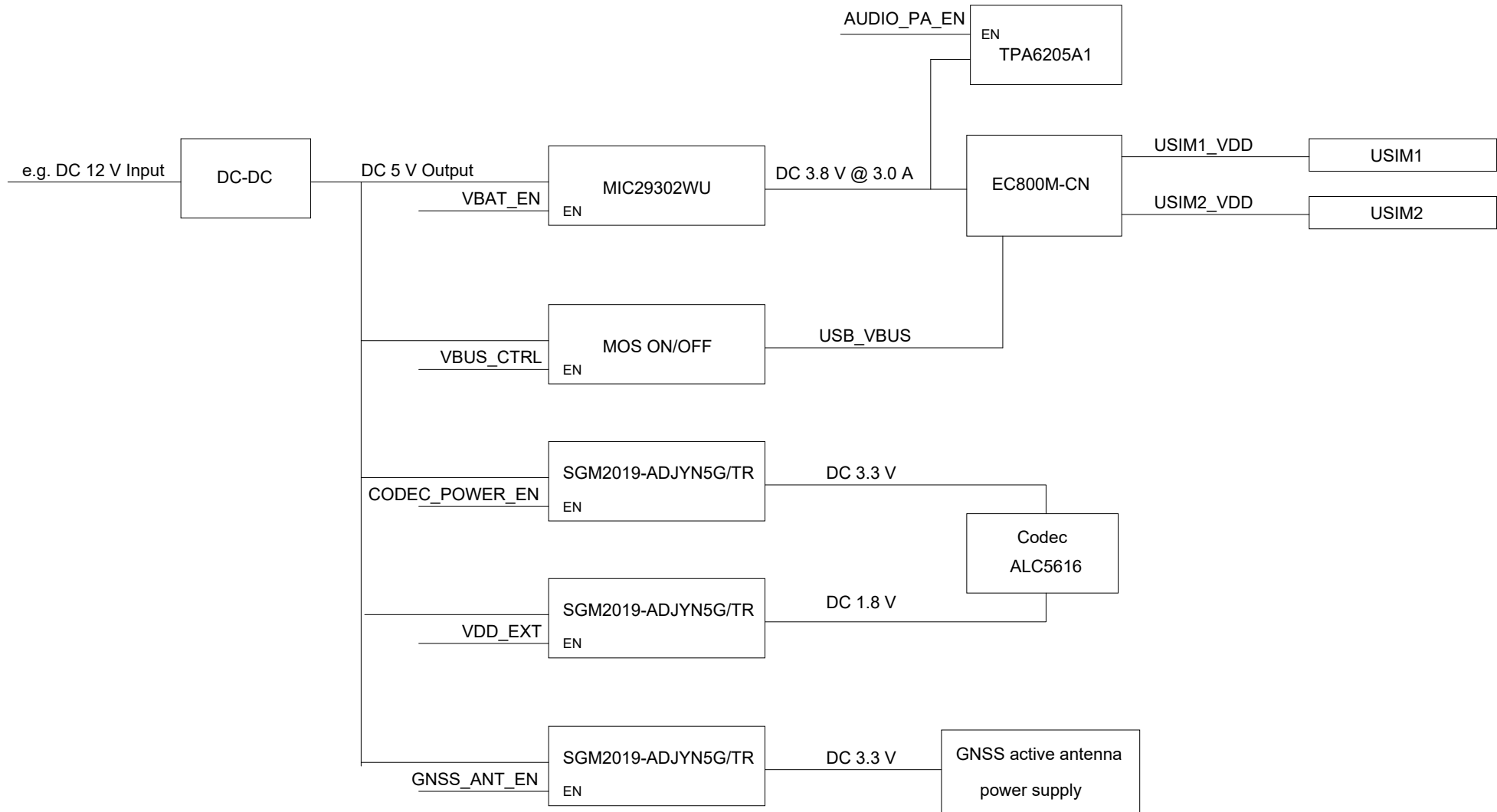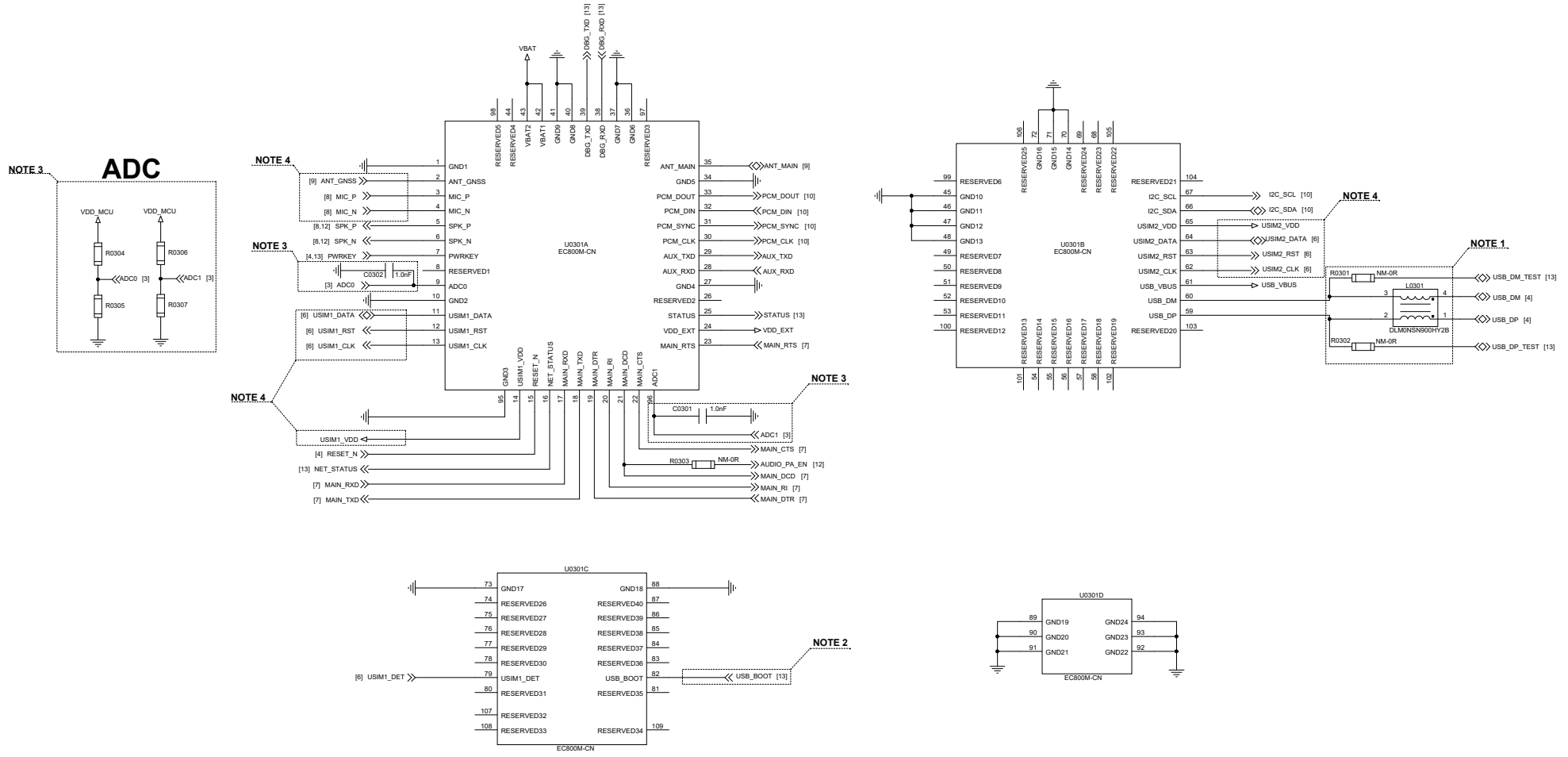
- VBAT → 3.8 V/ 2.0 A → VBAT

NOTE:

1. A level-shifting circuit or a voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.

2. GNSS function of the module is optional.

a) If both GNSS and analog audio input function are selected, the module requires an external microphone bias circuit. And MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO. Only USIM1 interface is supported on this condition.

b) If GNSS function is not selected but analog audio input function is needed, the module requires no external microphone bias circuit. And dual USIM cards are supported in this situation.

3. PCM, I2C and analog audio functions are all optional.

Power System Block Diagram

e.g. DC 12 V Input — **DC-DC** — DC 5 V Output

MIC29302WU — VBAT_EN / EN — DC 3.8 V @ 3.0 A — **EC800M-CN**

AUDIO_PA_EN — EN — **TPA6205A1**

EC800M-CN — USIM1_VDD — **USIM1**

EC800M-CN — USIM2_VDD — **USIM2**

MOS ON/OFF — VBUS_CTRL / EN — USB_VBUS

SGM2019-ADJYN5G/TR — CODEC_POWER_EN / EN — DC 3.3 V — **Codec ALC5616**

SGM2019-ADJYN5G/TR — VDD_EXT / EN — DC 1.8 V

SGM2019-ADJYN5G/TR — GNSS_ANT_EN / EN — DC 3.3 V — **GNSS active antenna power supply**

Module Interface

ADC

NOTE 3

VDD_MCU   VDD_MCU

R0304   R0306

ADC0 [3]   ADC1 [3]

R0305   R0307

NOTE 4

[9] ANT_GNSS
[8] MIC_P
[8] MIC_N
[8,12] SPK_P
[8,12] SPK_N
[4,13] PWRKEY

NOTE 3

C0302 1.0nF
[3] ADC0

[6] USIM1_DATA
[6] USIM1_RST
[6] USIM1_CLK

U0301A
EC800M-CN

1 GND1	ANT_MAIN 35 → ANT_MAIN [9]
2 ANT_GNSS	GND5 34
3 MIC_P	PCM_DOUT 33 → PCM_DOUT [10]
4 MIC_N	PCM_DIN 32 ← PCM_DIN [10]
5 SPK_P	PCM_SYNC 31 → PCM_SYNC [10]
6 SPK_N	PCM_CLK 30 → PCM_CLK [10]
7 PWRKEY	AUX_TXD 29 → AUX_TXD
8 RESERVED1	AUX_RXD 28 ← AUX_RXD
9 ADC0	GND4 27
10 GND2	RESERVED2 26
11 USIM1_DATA	STATUS 25 → STATUS [13]
12 USIM1_RST	VDD_EXT 24 → VDD_EXT
13 USIM1_CLK	MAIN_RTS 23 ← MAIN_RTS [7]

VBAT

DBG_TXD [13]
DBG_RXD [13]

98 RESERVED5
44 RESERVED4
43 VBAT2
42 VBAT1
41 GND9
40 GND8
39 DBG_TXD
38 DBG_RXD
37 GND7
36 GND6
97 RESERVED3

95 GND3
14 USIM1_VDD
15 RESET_N
16 NET_STATUS
17 MAIN_RXD
18 MAIN_TXD
19 MAIN_DTR
20 MAIN_RI
21 MAIN_DCD
22 MAIN_CTS
96 ADC1

NOTE 3

C0301 1.0nF
ADC1 [3]

R0303 NM-0R

MAIN_CTS [7]
AUDIO_PA_EN [12]
MAIN_DCD [7]
MAIN_RI [7]
MAIN_DTR [7]

USIM1_VDD

[4] RESET_N
[13] NET_STATUS
[7] MAIN_RXD
[7] MAIN_TXD

NOTE 4

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106 RESERVED25
72 GND16
71 GND15
70 GND14
69 RESERVED24
68 RESERVED23
105 RESERVED22

U0301B
EC800M-CN

99 RESERVED6	RESERVED21 104
45 GND10	I2C_SCL 67 → I2C_SCL [10]
46 GND11	I2C_SDA 66 → I2C_SDA [10]
47 GND12	USIM2_VDD 65 → USIM2_VDD
48 GND13	USIM2_DATA 64 ↔ USIM2_DATA [6]
49 RESERVED7	USIM2_RST 63 ← USIM2_RST [6]
50 RESERVED8	USIM2_CLK 62 ← USIM2_CLK [6]
51 RESERVED9	USB_VBUS 61 → USB_VBUS
52 RESERVED10	USB_DM 60
53 RESERVED11	USB_DP 59
100 RESERVED12	RESERVED20 103

101 RESERVED13
54 RESERVED14
55 RESERVED15
56 RESERVED16
57 RESERVED17
58 RESERVED18
102 RESERVED19

NOTE 4

NOTE 1

R0301 NM-0R
L0301
USB_DM_TEST [13]
USB_DM [4]
3   4
2   1
DLM0NSN900HY2B
USB_DP [4]
R0302 NM-0R
USB_DP_TEST [13]

U0301C

73 GND17	GND18 88
74 RESERVED26	RESERVED40 87
75 RESERVED27	RESERVED39 86
76 RESERVED28	RESERVED38 85
77 RESERVED29	RESERVED37 84
78 RESERVED30	RESERVED36 83
79 USIM1_DET	USB_BOOT 82
80 RESERVED31	RESERVED35 81
107 RESERVED32	
108 RESERVED33	RESERVED34 109

EC800M-CN

[6] USIM1_DET

NOTE 2
USB_BOOT [13]

U0301D

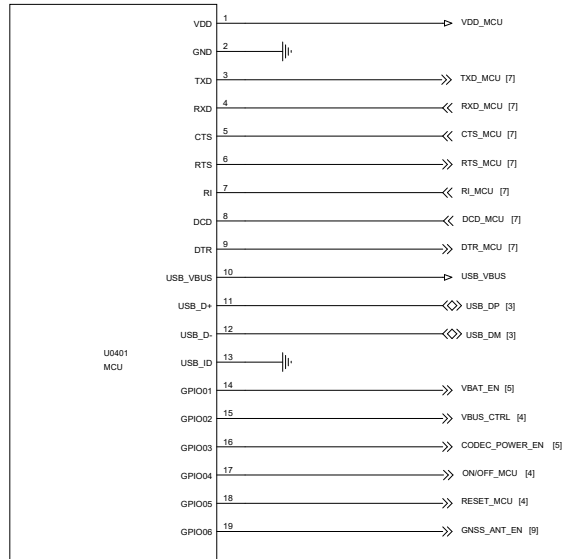|	
89 GND19	GND24 94
90 GND20	GND23 93
91 GND21	GND22 92

EC800M-CN

NOTE:

1. A common mode choke L0301 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission, and it
   should be placed close to the module. Meanwhile, it is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the extra
   stubs of the trace. The two resistors R0301 and R0302 should be placed close to the module to ensure the integrity of USB signal.
2. USB_BOOT cannot be pulled down to low level before the module starts up successfully.
3. The voltage input range of ADC0 and ADC1 is 0–1.2 V. A voltage divider with resistance of more than 100 kΩ must be used for ADC interface application.
   The accuracy of the two resistors in each voltage divider affects the sampling error of the ADC. It is recommended to use resistors with an accuracy of 1%; if the accuracy of the ADC needs to be higher, resistors with an accuracy of 0.5% are recommended.
4. GNSS function of the module is optional.
   a) If both GNSS and analog audio input function are selected, the module requires an external microphone bias circuit. And MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO. Only USIM1 interface is supported on this condition.
   b) If GNSS function is not selected but analog audio input function is needed, the module requires no external microphone bias circuit. And dual USIM cards are supported in this situation.
5. PCM, I2C and analog audio functions are all optional.
6. All GND pins should be connected to the ground, and unused and RESERVED pins are kept floated.
7. Ensure there is a complete reference ground plane below the module, and the gound plane should be placed close to the module layer as possible.
   Other traces cannot be routed on the first layer below the module, at least four-layer board design is recommended.

MCU Interface

U0401
MCU

Pin	Signal	Net
1	VDD	VDD_MCU
2	GND	
3	TXD	TXD_MCU [7]
4	RXD	RXD_MCU [7]
5	CTS	CTS_MCU [7]
6	RTS	RTS_MCU [7]
7	RI	RI_MCU [7]
8	DCD	DCD_MCU [7]
9	DTR	DTR_MCU [7]
10	USB_VBUS	USB_VBUS
11	USB_D+	USB_DP [3]
12	USB_D-	USB_DM [3]
13	USB_ID	
14	GPIO01	VBAT_EN [5]
15	GPIO02	VBUS_CTRL [4]
16	GPIO03	CODEC_POWER_EN [5]
17	GPIO04	ON/OFF_MCU [4]
18	GPIO05	RESET_MCU [4]
19	GPIO06	GNSS_ANT_EN [9]

It is used to turn on/off the module.

[4] ON/OFF_MCU

Q0403
DTC043ZEBTL

PWRKEY [3,13]

C0402
10nF

It is used to reset the module.

[4] RESET_MCU

Q0404
DTC043ZEBTL

RESET_N [3]

5 V power supply from motherboard.

DC_5V

Q0401

USB_VBUS

C0401
470nF

R0402
100K

R0401 10K

[4] VBUS_CTRL

Q0402
DTC043ZEBTL
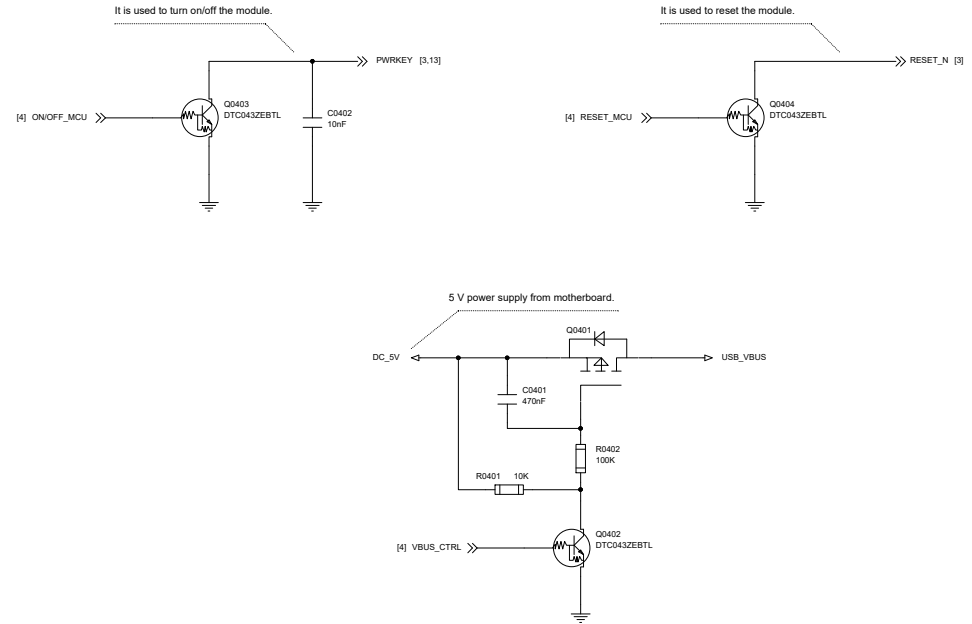
NOTE:

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V. If the power domain of GPIO interfaces of U0401 is also 1.8 V, then the related level-shifting circuit is not needed.

2. The USB interface of the module can only serves as a slave device and supports full-speed and high-speed modes of USB 2.0. To communicate with the USB interface, MCU needs to support USB host mode or OTG function.

   The USB_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.

3. It is recommended to select the GPIO pins which are at low level by default of MCU as the control pins for PWRKEY and RESET_N of the module. Please ensure that the load capacitance does not exceed 10 nF on PWRKEY and RESET_N pins.

Power Supply Design

DC-DC Application

When the input voltage is above 7.0 V, use a DC-DC converter to convert the high input voltage to a 5.0 V output, and then use LDOs to convert it to 3.8 V, 3.3 V and 1.8 V to power the module, aduio PA and Codec up.
The supply current of the module must meet 2.0 A.

e.g. DC 12 V Input → DC-DC → DC 5 V Output → LDO1 → DC 3.8 V Output → EC800M-CN / TPA6205A1

LDO2 → DC 3.3 V Output → Codec

LDO3 → DC 1.8 V Output → Codec

VBAT Design

VBAT

Close to VBAT pins.

D0501 WS4.5D3HV
C0502 100uF
C0512 100nF
C0501 33pF
C0509 10pF
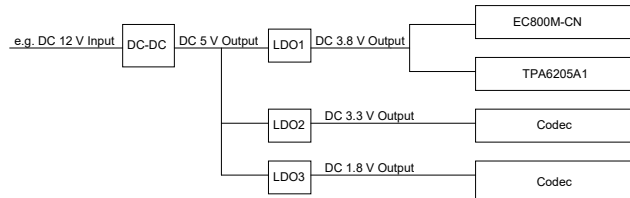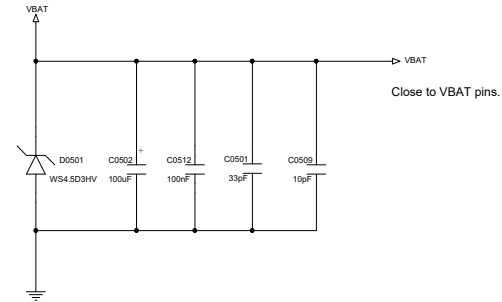
NOTE:

1. The power supply should be able to provide sufficient current up to 2.0 A for the module.

2. The width of VBAT trace should be not less than 2 mm.

3. The typical operating voltage of VBAT is 3.8 V.

LDO Application

When the input voltage is below 7.0 V, use an LDO to convert the input voltage to 3.8 V.

U0503 MIC29302WU

DC_5V

$VBAT = (R0507 / R0503 + 1) \times 1.24 = 3.88$ V

C0504 470uF
C0514 100nF
R0505 51K
R0507 100K +/-1%
C0522 470uF
C0516 100nF
R0511 330R
R0503 47K +/-1%

NOTE

[4] VBAT_EN

Q0501 DTC043ZEBTL
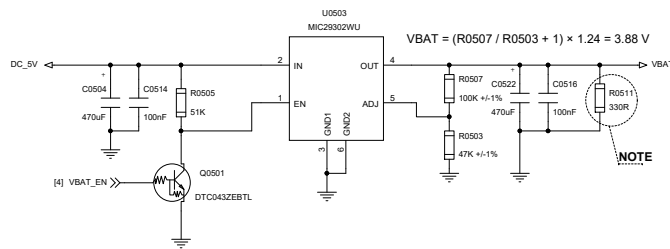
NOTE:
The recommended load current should be larger than 10 mA.

Power Supply for Codec

U0502 SGM2019-ADJYN5G/TR

DC_5V

$VDD\_3V3 = 1.207 \times (1 + R0504 / R0509) = 3.3$ V → VDD_3V3

C0513 1uF
C0511 100nF
DTC043ZEBTL Q0502
R0510 10K
R0504 73.2K +/-1%
C0521 4.7uF
C0518 100nF
C0507 33pF
R0509 42.2K +/-1%

[4] CODEC_POWER_EN

VDD_1V8

U0501 SGM2019-ADJYN5G/TR

DC_5V

$VDD\_1V8 = 1.207 \times (1 + R0501 / R0508) = 1.8$ V → VDD_1V8

C0503 1uF
C0505 100nF
R0502 0R
R0506 100K
R0501 39K +/-1%
C0510 4.7uF
C0515 100nF
C0517 33pF
R0508 75K +/-1%

VDD_EXT

NOTE:

1. VDD_EXT and CODEC_POWER_EN are used to turn on/off VDD_1V8 and VDD_3V3 respectively.

2. The following power-up/down sequences should be followed to ensure the audio codec works normally.

   Power-up sequence: power up VDD_1V8 first, and then VDD_3V3.

   Power-down sequence: power down VDD_3V3 first, and then VDD_1V8.

USIM Interfaces Design

USIM1

USIM2
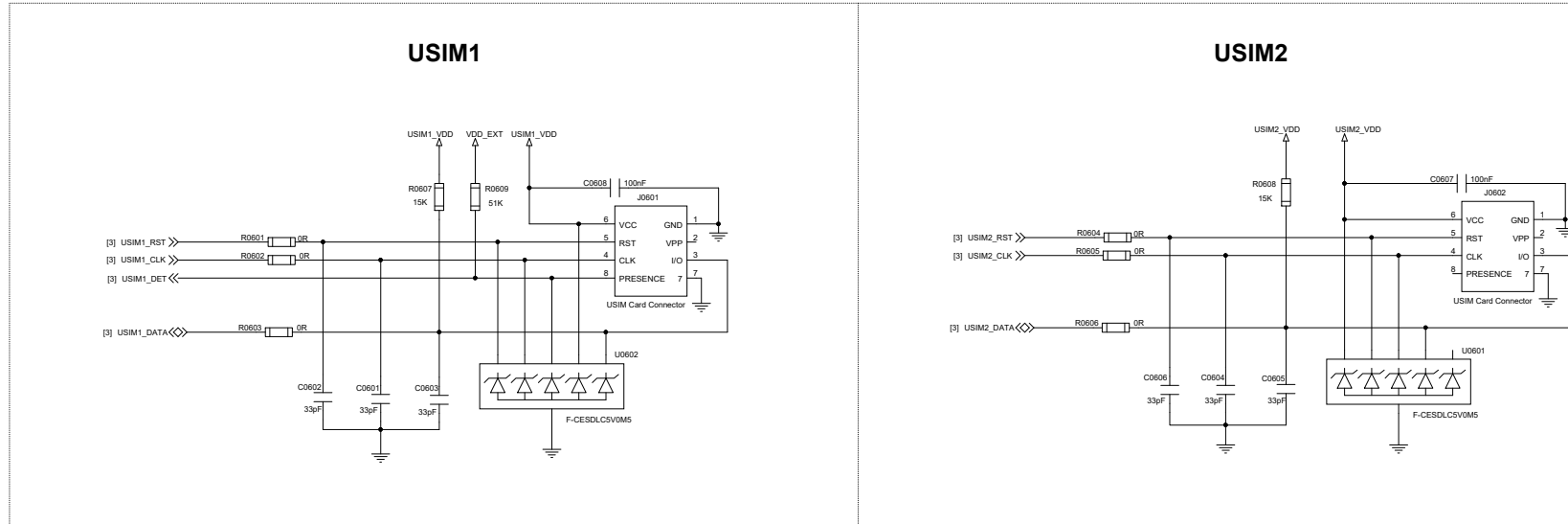
NOTE:

1. U0601 and U0602 are recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.

2. The pull-up resistors R0607 and R0608 can improve anti-jamming capability, and should be placed close to the USIM card connector.

3. R0601–R0606 are used for debugging, and C0601–C0606 are used for filtering out RF interference.

4. The capacitance of C0607 and C0608 should be less than 1 μF and they should be placed close to the USIM card connector.

5. If GNSS function is selected, only USIM1 interface is supported. If GNSS function is not selected, dual cards are supported.

UART Interface Design

UART Level-shifting Circuit - Transistor Solution
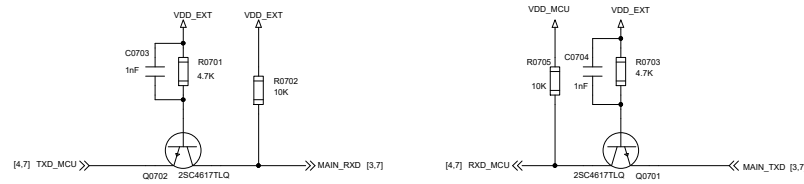
UART Level-shifting Circuit - IC Solution
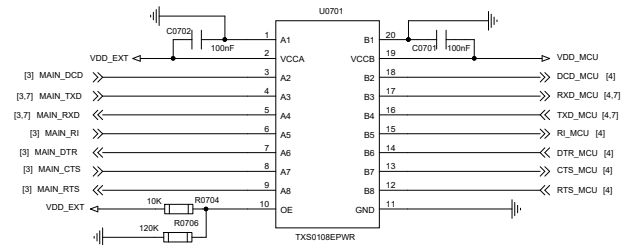
NOTE:

1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter one.

2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, please refer to the datasheet of TXS0108EPWR.

3. The transistor solution is not suitable for applications with high baud rates exceeding 460 kbps.The capacitors C0703 and C0704 of 1 nF can improve the signal quality.

4. MAIN_RTS and MAIN_DTR level-shifting circuits are similar to that of the MAIN_RXD.

   MAIN_CTS, MAIN_RI and MAIN_DCD level-shifting circuits are similar to that of the MAIN_TXD.

Analog Audio Design

Microphone Bias Circuit

NOTE1

MIC_BIAS

100nF C0821
R0803 510R

C0822 2.2uF
R0804 1.5K

[3] MIC_P — C0823 100nF — MIC_P_R [8]
R0801 0R

R0802 0R
[3] MIC_N — C0824 100nF — MIC_N_R [8]
R0805 1.5K

R0806 510R
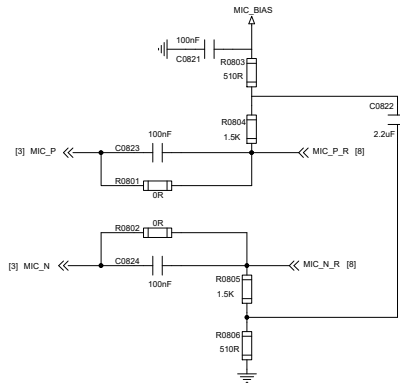
Case	C0821/C0822/C0823/C0824 R0803/R0804/R0805/R0806	R0801/R0802
External microphone bias circuit	M	NM
Without external microphone bias circuit	NM	M

Microphone Application

Close to microphone interface

C0803 10pF   C0812 33pF   D0803
[8] MIC_P_R
C0802 10pF   C0810 33pF
[8] MIC_N_R
C0814 10pF   C0805 33pF   D0802

J0802 MIC

Handset Application

Close to handset interface

C0819 10pF   C0804 33pF   C0801 10pF   C0820 33pF   C0809 10pF   C0808 33pF   D0804   D0801

[8] MIC_P_R — 0R B0801 4
[8] MIC_N_R — 0R B0804 1
[3,12] SPK_P — 0R B0803 3
[3,12] SPK_N — 0R B0802 2

C0813 10pF   C0811 33pF   C0806 10pF   C0818 33pF   C0816 10pF   C0815 33pF   D0806   D0805

J0801 HANDSETCON

NOTE:

1. The analog audio function is optional.

    a) If analog audio function is selected and GNSS function is also needed, the analog audio input interface requires an external microphone bias circuit.

    MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO.

    b) When GNSS function is not needed, the analog audio input interface requires no external microphone bias circuit.

2. Both the MIC and SPK signal traces need to be routed as differential pairs.

3. All MIC and SPK signal traces should be surrounded with ground on the layer and ground planes above and below, and far away from noises.

4. In the audio design, you can choose either the analog audio or the codec. It is not necessary to select both.

5. It is recommended to use 10 pF and 33 pF capacitors to filter TDD noise.

Antenna Interface Design

GNSS Active Antenna Power Supply

DC_5V

U0901
SGM2019-ADJYN5G/TR

GNSS_VDD_3V3 = 1.207 × (1 + R0907 / R0905) = 3.3 V

IN 1
OUT 5
EN 3
GND 2
FB 4

C0909 1uF
C0908 100nF
DTC043ZEBTL
Q0901
R0906 10K
R0907 73.2K +/-1%
R0905 42.2K +/-1%
C0910 4.7uF
C0907 100nF
C0906 33pF

GNSS_VDD_3V3

[4] GNSS_ANT_EN
VDD_1V8

Main Antenna Design

J0901

NOTE 5

R0902 0R

ANT_MAIN [3]

C0903 NM
C0904 NM

GNSS Antenna Design

GNSS_VDD_3V3

NOTE 2 & 3

C0901
100nF +/-10% 10V
R0903 10R +/-5% 1/16W

L0901 47nH +/-5%

J0902

C0911
100pF +/-5% 50V

D0901
GESD1005H5R5CR10GPT

NOTE 4

R0904 0R

ANT_GNSS [3]

C0902 NM
C0905 NM

NOTE 5

NOTE:

1. GNSS function is optional to the module. Thus, the GNSS antenna design of this page is only applicable to the variant with built-in GNSS function.

2. The active antenna uses an LDO for power supply, and when using passive antenna, the VDD circuit is not needed.

3. L0901, R0903, C0901 are recommended to be placed close to the RF traces in layout design.

4. The junction capacitance of the antenna interface ESD protection component is recommended to be less than 0.05 pF.

5. Reserve a Π-type matching circuit at antenna interface.

6. The single-ended impedance of the RF antenna is 50 Ω, and length should be as short as possible.

7. The external active antenna power supply voltage range is from 2.8 V to 4.3 V, and the typical value is 3.3 V.

   The power supply voltage can be designed according to the power supply requirements of the selected active antenna.
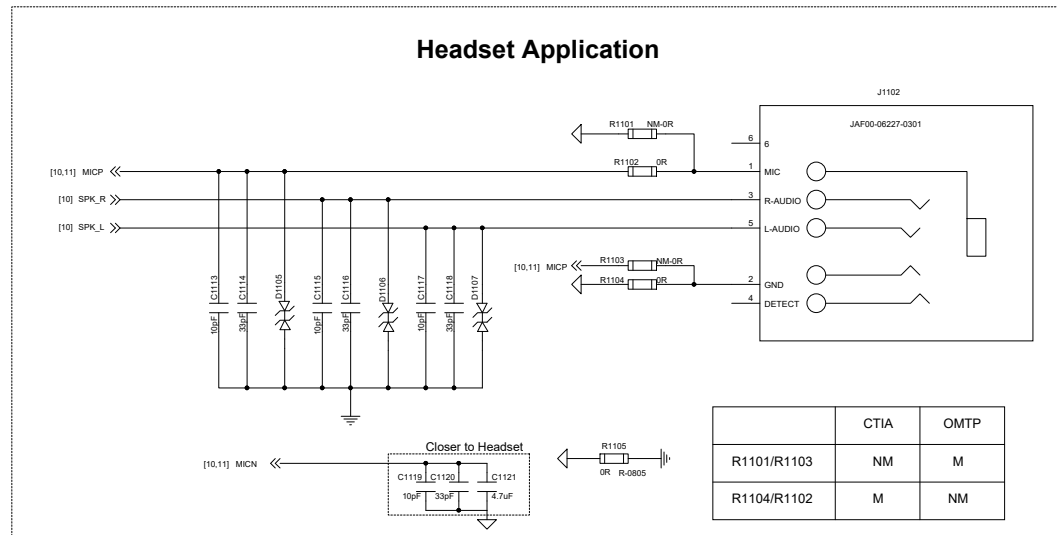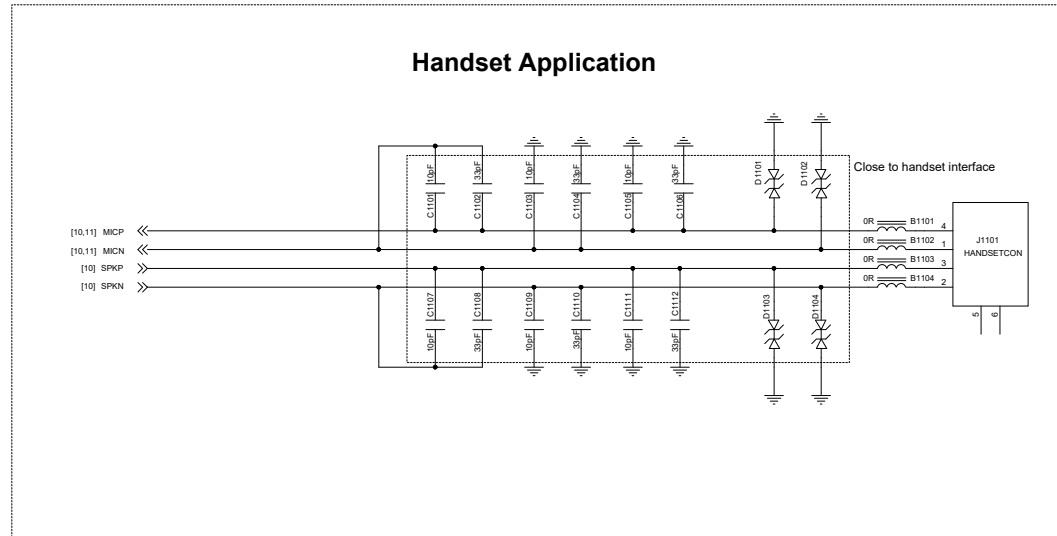
Audio Codec Design (ALC5616)
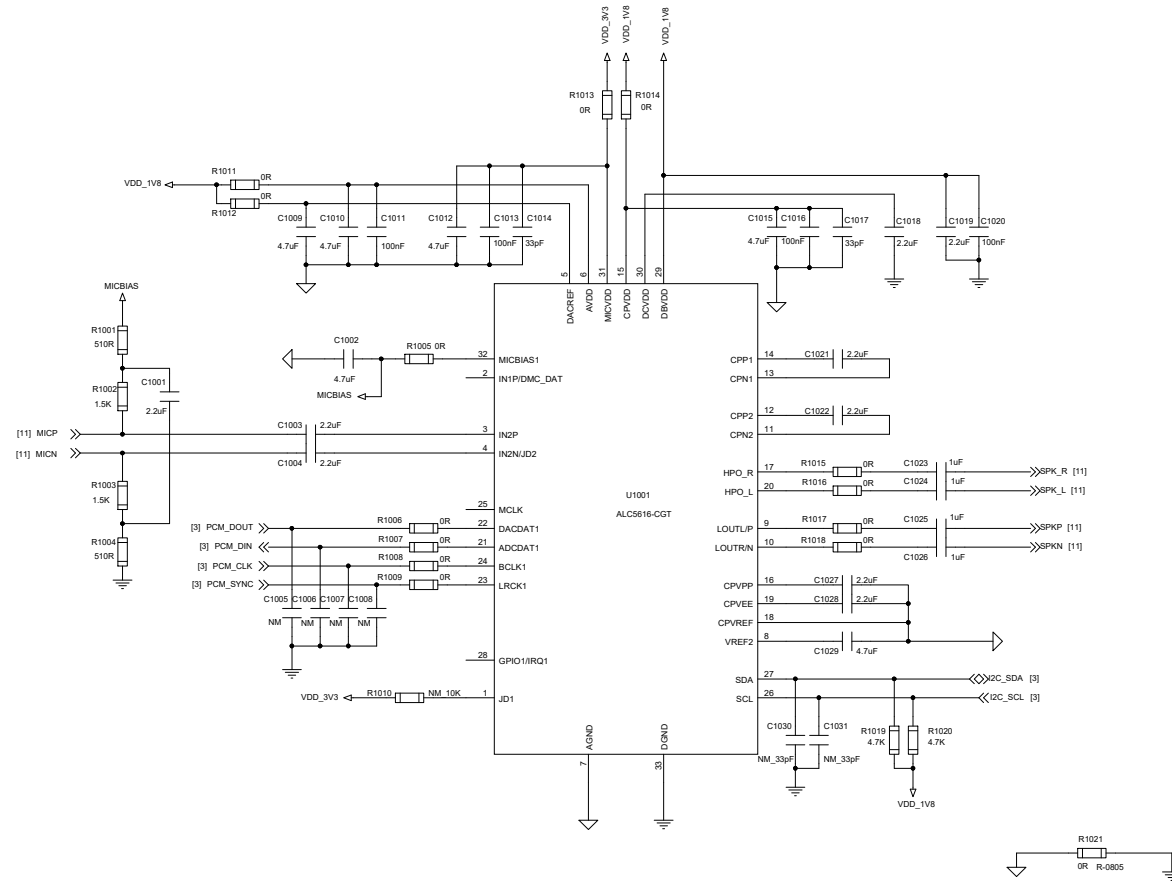
NOTE:

1. ALC5616 power-up sequence: DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD → MICVDD → software initialization.

2. ALC5616 power-down sequence: disable Codec function by software → MICVDD → DBVDD/I2C pull-up power/AVDD/DACREF/CPVDD.

3. The module will automatically initialize the Codec via I2C interface after it is turned on successfully, so all power supplies for the Codec need to be powered up before that.

4. Please pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with a 0 Ω resistor packaged as R-0805. For more details, please refer to sheet "Audio Codec Interface Design".

5. For more details, please refer to the datasheet of ALC5616.

6. The analog audio function is optional. If those interfaces are not used, keep them floated.

Audio Codec Interface Design

Handset Application

Close to handset interface

Headset Application

|	CTIA	OMTP
R1101/R1103	NM	M
R1104/R1102	M	NM

NOTE:

1. The Codec analog output can drive handset and headset. For larger power loads such as loudspeaker, an audio power amplifier should be added in the design.

2. In handset applications, route the MIC and SPK signal traces as differential pairs respectively.

3. In headset applications, route the MIC signal traces as a differential pair.

4. All MIC and SPK signal traces shall be surrounded with ground on the layer and ground planes above and below, and far away from noises such as clock and DC-DC signals.

5. Please pay attention to the distinction between analog ground and digital ground. The analog ground and digital ground need to be connected with 0 Ω resistor

   packaged as R-0805 (short-circuit through single point grounding).

6. The analog audio function is optional. If those interfaces are not used, keep them floated.

Analog Audio Design (Audio Power Amplifier)
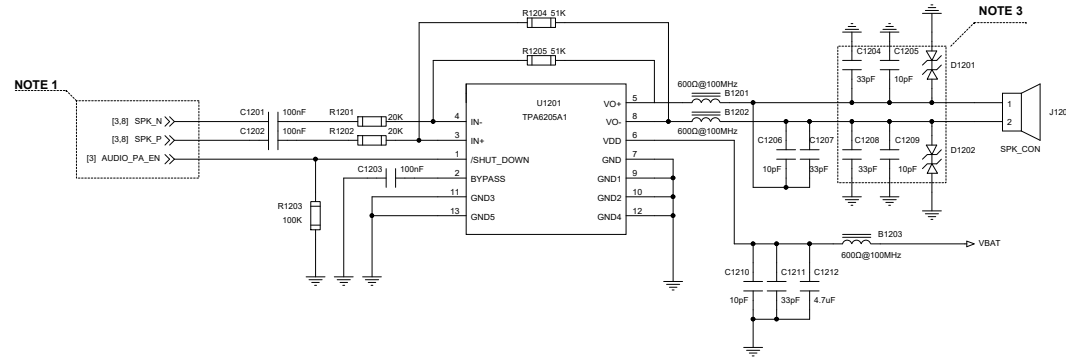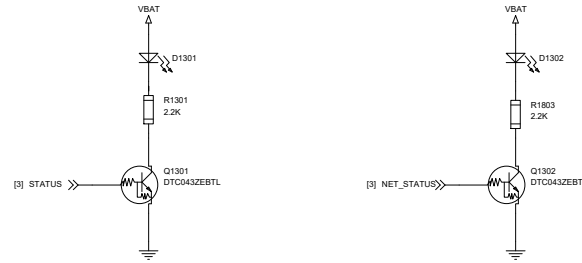

NOTE:

1. SPK_P and SPK_N are differential output channels that can be used for an external audio power amplifier.

   It is recommended to use MAIN_DCD of the module to control the enable pin of the audio power amplifier to eliminate POP. For more information about AUDIO_PA_EN, please contact Quectel Technical Support.

2. The power amplifier above is for reference only. Select the appropriate audio power amplifier according to actual needs.

3. Filter capacitors and ESD protection components should be placed close to the loudspeaker.

4. The selection of ESD protection components is related to the selection of audio power amplifier. Please ensure that the output voltage of audio power amplifier is

   within the maximum reverse working voltage range of ESD protection components under normal working condition, so as to avoid damage to ESD protection components.

5. The analog audio function is optional. If those interfaces are not used, keep them floated.

Other Designs

Indicators

VBAT

D1301

R1301
2.2K

Q1301
DTC043ZEBTL

[3] STATUS
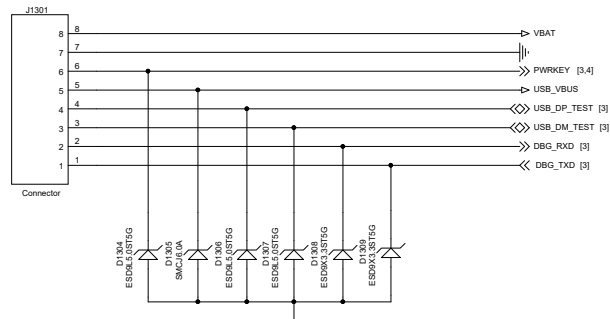
VBAT

D1302

R1803
2.2K

Q1302
DTC043ZEBTL

[3] NET_STATUS

NOTE:

1. For more details about STATUS and NET_STATUS, please refer to the hardware design document of the module.

2. If the low current consumption is required when your device is in sleep mode, replace the power supply VBAT of the STATUS and

NET_STATUS indicators with the external controllable ones, which can be turned off when the module is in sleep mode to reduce the power consumption.
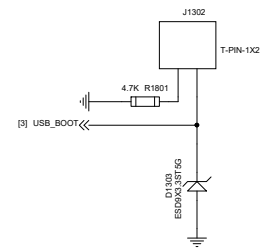
Reserved Test Points

J1301

8	8	VBAT
7	7	
6	6	PWRKEY [3,4]
5	5	USB_VBUS
4	4	USB_DP_TEST [3]
3	3	USB_DM_TEST [3]
2	2	DBG_RXD [3]
1	1	DBG_TXD [3]

Connector

D1304 ESD9L5.0ST5G
D1305 SMCJ6.0A
D1306 ESD9L5.0ST5G
D1307 ESD9L5.0ST5G
D1308 ESD9X3.3ST5G
D1309 ESD9X3.3ST5G

NOTE:

1. Test points for both USB and debug UART interfaces are reserved for catching logs.

2. Test points for USB interface can also be reserved for firmware upgrade.

3. The junction capacitance of the ESD protection componets on USB data lines should be less than 2 pF.

4. The debug UART interface supports 1.8 V power domain, and a voltage-level translator should be used

if the power domain of your application is 3.3 V.

USB_BOOT Interface

J1302

T-PIN-1X2

4.7K R1801

[3] USB_BOOT

D1303 ESD9X3.3ST5G

NOTE:

1. Be sure to reserve the USB_BOOT interface design and test points.

2. Before module is turned on, pull down USB_BOOT to GND, and the module will enter emergency download mode

when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

3. The 6.0.1 and above version of Qflash tool must be used for firmware upgrading.