EC800M-CN

Hardware Design

LTE Standard Module Series

Version: 1.0

Date: 2022-09-20

Status: Released

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-08-19	Kelly WANG/Janko LI/ Yule DENG	Creation of the document
1.0	2022-09-20	Kelly WANG/Janko LI/ Yule DENG	First official release

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1 Introduction

This document defines the EC800M-CN module and describes its air interface and hardware interfaces which are connected with your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

The module is an SMD type module with compact packaging, which is engineered to meet the demands in M2M and IoT applications, for instance:

- OTT
- CPE
- POS
- Tracker
- Data card
- Security system
- Industrial PDA

Table 2: Basic Information

EC800M-CN	
Packaging type	LCC + LGA
Pin counts	109
Dimensions	(17.7 ±0.15) mm × (15.8 ±0.15) mm × (2.4 ±0.2) mm
Weight	approx. 1.4 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Wireless Network Type	EC800M-CN
LTE-FDD	B1/B3/B5/B8
LTE-TDD	B34/B38/B39/B40/B41
GNSS (optional)	GPS/BDS/Galileo/GLONASS

NOTE

GNSS function of the module is optional.

- If both GNSS and analog audio input function are selected, the module requires an external microphone bias circuit. And MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO. Only USIM1 interface is supported on this condition.
- If GNSS function is not selected but analog audio input function is needed, the module requires no external microphone bias circuit. And dual USIM cards are supported in this situation.

2.2. Key Features

Table 4: Key Features

Categories	Descriptions
Supply Voltage	● Supply voltage range: 3.4–4.3 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: stored in USIM card and ME, ME by default ● SGS SMS (default), IMS SMS (optional)
USIM Interface	Supports 1.8 V and 3.0 V
Audio Features (optional)	● Supports one digital audio interface: PCM interface ● Supports one analog audio input and one analog audio output ● Supports echo cancellation and noise suppression
PCM Interface (optional)	● Used for audio data transmission with external Codec ● Supports 16-bit linear data format ● Supports short frame synchronization: the module only works as a master device
I2C Interface (optional)	● Supports one I2C interface ● Complies with I2C-bus specification
USB Interface	● Compliant with USB 2.0 (slave mode only), with data transmission rates up to 480 Mbps ● Used for AT command communication, data transmission, GNSS NMEA message output, software debugging and firmware upgrade ● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–5.18 and Android 4.x–12.x
UART	**Main UART:** ● Used for AT command communication and data transmission

	● Baud rate: 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for log output and GNSS NMEA message output ● Baud rate: 115200 bps **Auxiliary UART*:** ● Used for communication with peripherals ● Baud rate: 115200 bps
Network Indication	NET_STATUS: indicates network registration status
AT Commands	Compliant with *3GPP TS 27.007, 3GPP TS 27.005* and Quectel enhanced AT commands
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● GNSS antenna interface (ANT_GNSS) (optional) ● 50 Ω characteristic impedance
Transmitting Power	● LTE-FDD: Class 3 (23 dBm ±2 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports Cat 1 FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● LTE-FDD maximum data rates: – DL: 10 Mbps – UL: 5 Mbps ● LTE-TDD maximum data rates: – DL: 8.96 Mbps – UL: 3.1 Mbps
Position Fixing	● Supports Wi-Fi Scan (share the main antenna) ● Supports GNSS positioning (optional)
Internet Protocol Features	● Compliant with TCP, UDP, PPP, NTP, NITZ, FTP, HTTP, PING, CMUX*, HTTPS, FTPS, SSL, FILE, MQTT, MMS*, SMTP* and SMTPS* protocols ● Compliant with PPP protocol's PAP and CHAP authentication
Temperature Ranges	● Normal operating temperature [1]: -35 °C to +75 °C ● Extended temperature [2]: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	Use USB 2.0 interface or DFOTA to upgrade
RoHS	All hardware components are fully compliant with EU RoHS directive

[1] Within this range, the module's related performance can meet 3GPP specifications.
[2] Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call*, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

NOTE

The 6.0.1 and above version Qflash tool must be used for firmware upgrade.

2.3. Functional Diagram

The block diagram illustrates the following major functional parts:

- Power management
- Baseband part
- Flash
- Radio frequency part
- Peripheral interfaces

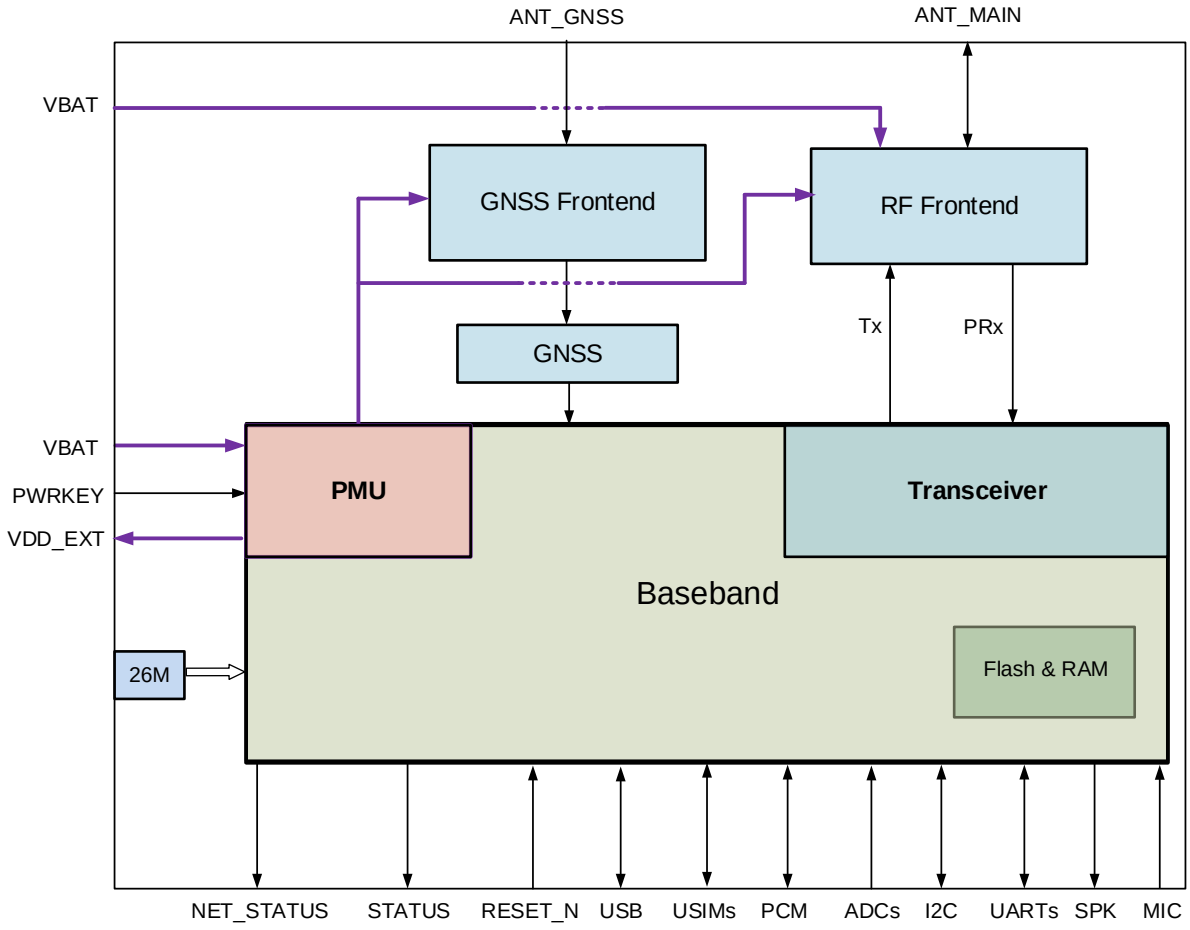


Figure 1: Functional Diagram

2.4. Pin Assignment

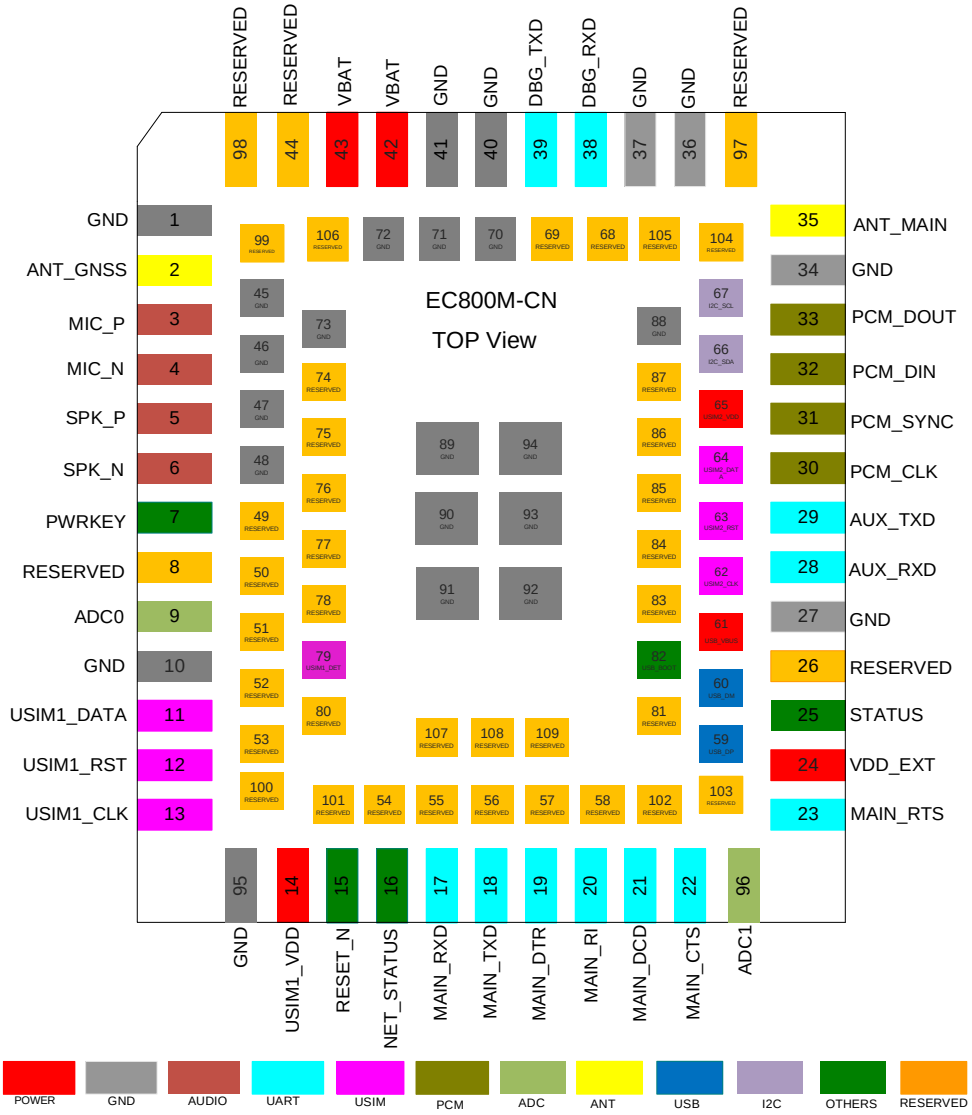


Figure 2: Pin Assignment (Top View)

NOTE

1. GNSS function of the module is optional.
   - If both GNSS and analog audio input functions are selected, the module requires an external microphone bias circuit. And MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO. Only USIM1 interface is supported on this condition.
   - If GNSS function is not selected but analog audio input function is needed, the module requires no external microphone bias circuit. And dual USIM cards are supported in this situation.

2. PCM, I2C and analog audio functions are all optional. If those interfaces are not used, keep them floated.
3. Keep all RESERVED pins and unused pins floated.
4. Do not pull USB_BOOT to low level before the module is successfully turned on.
5. Ensure there is a complete reference ground plane under the module and the plane shall be placed as close to the module-layer as possible. There will be no other traces on the first layer under the module. And at least four-layer design is recommended.
6. The 6.0.1 and above version Qflash tool must be used for firmware upgrading.

2.5. Pin Description

Table 5: Parameter Definition

Parameters	Descriptions
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 6: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	42, 43	PI	Power supply for the module	Vmax = 4.3 V Vmin = 3.4 V Vnom = 3.8 V	External power supply must be provided with sufficient current up

					to 2.0 A. It is recommended to add a TVS diode externally.
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95				
Power Supply Output					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_EXT	24	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. If unused, keep it open.
Turn on/off/Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Turn on/off the module	V_{IL}max = 0.5 V Vnom = VBAT	Pull down PWRKEY for at least 700 ms to turn on/off the module.
RESET_N	15	DI	Reset the module	V_{IL}max = 0.5 V Vnom = 1.8 V	Active Low. If unused, keep it open.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_STATUS	16	DO	Indicate the module's network activity status	1.8 V	If unused, keep them open.
STATUS	25	DO	Indicate the module's operation status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	59	AIO	USB differential data (+)		Complies with USB 2.0. A differential impedance of 90 Ω is needed. If unused, keep them open.
USB_DM	60	AIO	USB differential data (-)		

USB_VBUS	61	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	If unused, keep it open.
USIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DATA	11	DIO	USIM1 card data	1.8/3.0 V	
USIM1_RST	12	DO	USIM1 card reset		
USIM1_CLK	13	DO	USIM1 card clock		
USIM1_VDD	14	PO	USIM1 card power supply		Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM1_DET	79	DI	USIM1 card hot-swap detect	1.8 V	If unused, keep it open.
USIM2_VDD	65	PO	USIM2 card power supply	1.8/3.0 V	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM2_DATA	64	DIO	USIM2 card data		
USIM2_CLK	62	DO	USIM2 card clock		
USIM2_RST	63	DO	USIM2 card reset		
Auxiliary UART Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_RXD	28	DI	Auxiliary UART receive	1.8 V	If unused, keep them open.
AUX_TXD	29	DO	Auxiliary UART transmit		
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RXD	17	DI	Main UART receive	1.8 V	If unused, keep

MAIN_TXD	18	DO	Main UART transmit		them open.
MAIN_DTR	19	DI	Main UART data terminal ready		
MAIN_RI	20	DO	Main UART ring indication		
MAIN_DCD	21	DO	Main UART data carrier detection		
MAIN_CTS	22	DO	DTE clear to send signal from DCE		Connect to DTE's CTS. If unused, keep it open.
MAIN_RTS	23	DI	DTE request to send signal to DCE		Connect to DTE's RTS. If unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	38	DI	Debug UART receive	1.8 V	If unused, keep them open.
DBG_TXD	39	DO	Debug UART transmit		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SDA	66	OD	I2C serial data		An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SCL	67	OD	I2C serial clock		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	30	DO	PCM clock	1.8 V	If unused, keep them open.
PCM_SYNC	31	DO	PCM data frame sync		
PCM_DIN	32	DI	PCM data input		
PCM_DOUT	33	DO	PCM data output		
Analog Audio Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MIC_P	3	AI	Microphone analog input (+)		If unused, keep them open.
MIC_N	4	AI	Microphone analog input (-)		
SPK_P	5	AO	Analog audio differential output (+)		Used for earpiece. The interface can drive 32 Ω earpiece with power rate at 37 mW. It can also be used to drive external power amplifier devices if the output power rate cannot meet the demand. If unused, keep them open.
SPK_N	6	AO	Analog audio differential output (-)		
Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_GNSS	2	AI	GNSS antenna interface		50 Ω impedance. If unused, keep it open. It is optional for the module.
ANT_MAIN	35	AIO	Main antenna interface		50 Ω impedance.
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	9	AI	General-purpose ADC interface	1.2 V	If unused, keep them open.
ADC1	96	AI			
Other Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	82	DI	Force the module into emergency download mode	1.8 V	Active low. This pin cannot be pulled down to low level before the

		module starts up successfully. It is recommended to reserve test points.
RESERVED Pins		
Pin Name	**Pin No.**	**Comment**
RESERVED	8, 26, 44, 49–58, 68, 69, 74–78, 80, 81, 83–87, 97–109	Keep these pins open.

NOTE

1. GNSS function of the module is optional.
   - If both GNSS and analog audio input function are selected, the module requires an external microphone bias circuit. And MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO. Only USIM1 interface is supported on this condition.
   - If GNSS function is not selected but analog audio input function is needed, the module requires no external microphone bias circuit. And dual USIM cards are supported in this situation.
2. PCM, I2C and analog audio functions are all optional. If those interfaces are not used, keep them floated.
3. Keep all RESERVED pins and unused pins floated.
4. Do not pull USB_BOOT to low level before the module is successfully turned on.

2.6. EVB Kit

Quectel supplies an evaluation board (UMTS & LTE EVB) with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Overview of Operating Modes

Modes	Functions	
Full Functionality Mode	Idle	Software is active. The module is registered on the network but has no data interaction with the network.
	Voice/Data	Network connection is ongoing. Power consumption is decided by the network setting and data transmission rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to the minimum functionality mode when the power is on. In this case, both RF function and USIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	Power consumption of the module will be reduced to a minimal level. The module can still receive paging, SMS, voice call and TCP/UDP data from network.	
Power Down Mode	PMU shuts down the power supply. Software is not active and UART interfaces are not accessible. However, operating voltage connected to VBAT remains applied.	

NOTE

For more details about **AT+CFUN**, see ***document [2]***.

3.2. Sleep Mode

In sleep mode, power consumption of the module can be reduced to a minimal level. The following sub-chapters describe how to let the module enter sleep mode.

3.2.1. UART Application Scenario

If the module communicates with the host via MAIN_UART, both the following two preconditions should be met to set the module to enter sleep mode:

- Execute **AT+QSCLK=1**.
- Drive MAIN_DTR to high level or keep it open.

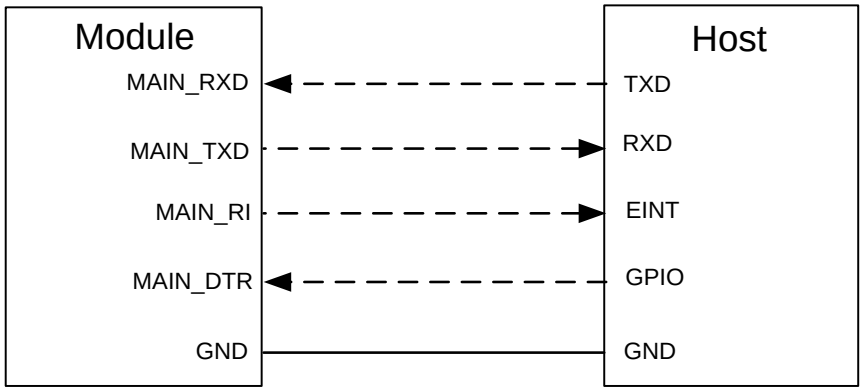


Figure 3: Block Diagram of UART Application in Sleep Mode

- You can wake up the module by driving MAIN_DTR low by the host.
- When the module has a URC to report, MAIN_RI signal will wake up the host. See ***Chapter 4.9.3*** for details about MAIN_RI.

3.2.2. USB Application Scenario

For the two situations (“USB application with USB remote wakeup function” and “USB application with USB suspend/resume and RI function”) below, three preconditions must be met to set the module into sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held at a high level or keep it open.
- Ensure the host’s USB bus, which is connected with the module’s USB interface, enters into suspend state.

3.2.2.1. USB Application with USB Remote Wakeup Function

The host supports USB suspend/resume and remote wakeup functions.

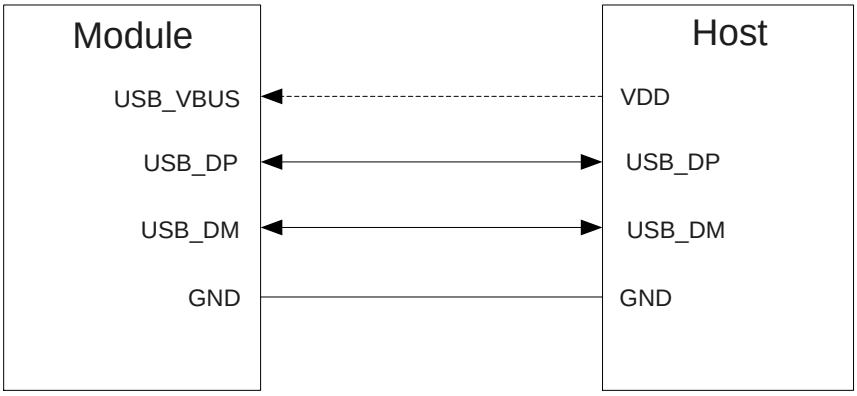


Figure 4: Block Diagram of Application with USB Remote Wakeup Function in Sleep Mode

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

3.2.2.2. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

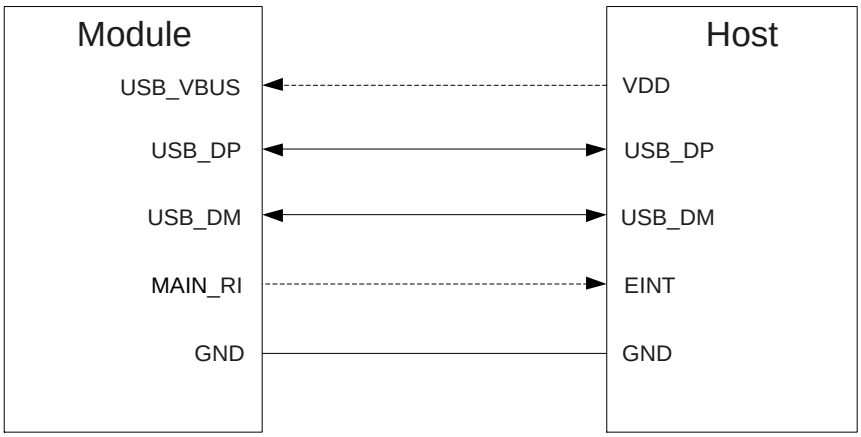


Figure 5: Block Diagram of Application with MAIN_RI Function in Sleep Mode

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will wake up the host through MAIN_RI signal. See ***Chapter 4.9.3*** for details about MAIN_RI.

3.2.2.3. USB Application without USB Suspend Function

If the host does not support USB suspend function, the following three preconditions must be met to let the module enter sleep mode:

- Execute **AT+QSCLK=1**.
- Drive MAIN_DTR to high level or keep it open.
- Disconnect USB_VBUS via the Power Switch.

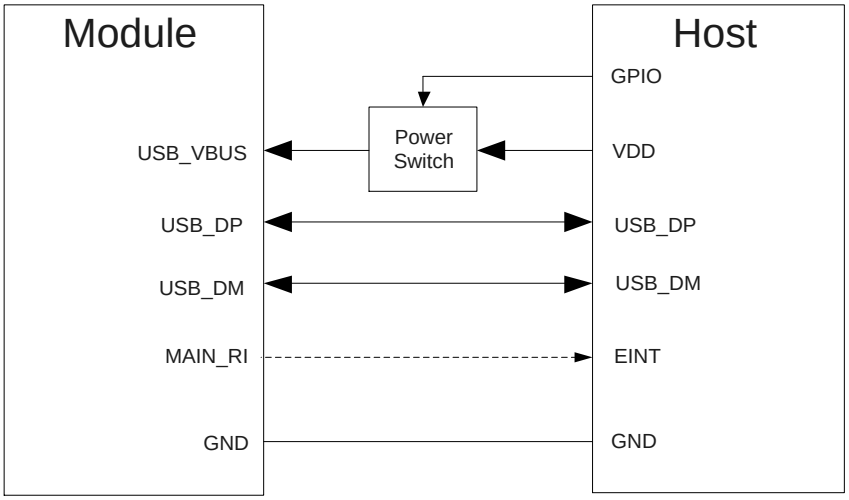


Figure 6: Block Diagram of Application without USB Suspend Function in Sleep Mode

Restore the power supply of USB_VBUS will wake up the module.

NOTE

1. Pay attention to the level matching represented by the dotted line between the module and the host.
2. For more details about AT commands, see ***document [2]***.

3.3. Airplane Mode

When the module enters into airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via following ways:

Software:

AT+CFUN=<fun> provides choices of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality (disable RF function and USIM function).
- **AT+CFUN=1:** Full functionality (default).
- **AT+CFUN=4:** Airplane mode (disable RF function).

NOTE

For more details about AT commands, see ***document [2]***.

3.4. Power Supply

3.4.1. Power Supply Interface

The module provides two VBAT pins dedicated for connection with the external power supply:

Table 8: Pin Description of Power Supply Interface

Pin Name	Pin No.	I/O	Description	Comment
VBAT	42, 43	PI	Power supply for the module	External power supply must be provided with sufficient current up to 2.0 A. It is recommended to add a TVS diode externally.
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95			

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 2 A. If the voltage difference between input voltage and the desired output VBAT is small, it is suggested to use an LDO; if the voltage difference is large, then a buck converter is suggested to use.

The following figure illustrates a reference design for 5 V input power supply, which adopts an MIC29302WU from Micrel.

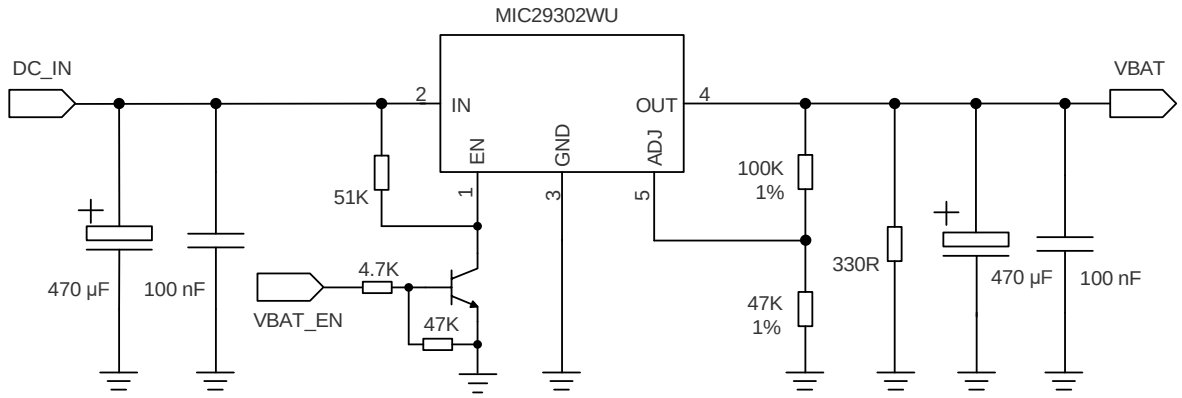


Figure 7: Reference Design of Power Input

NOTE

To avoid corrupting internal flash, do not cut off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.4 V to 4.3 V. Ensure the input voltage never drops below 3.4 V.

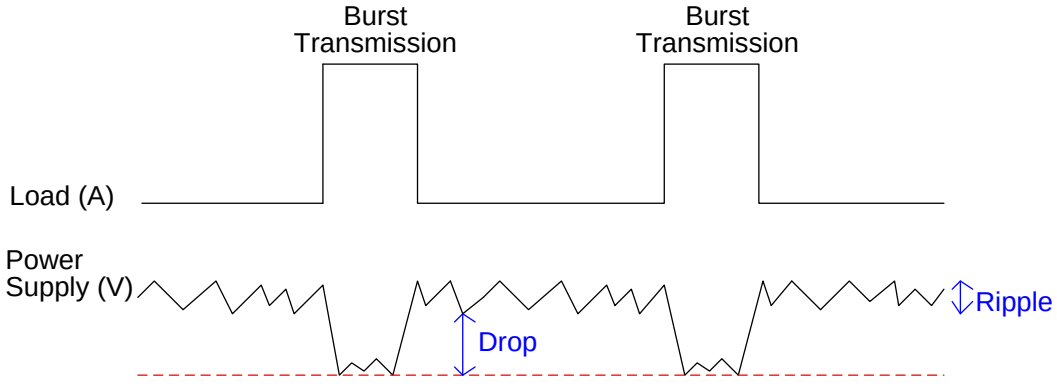


Figure 8: Power Supply Limits During Burst Transmission

To decrease the voltage drop, a bypass capacitor of about 100 µF with low ESR (ESR ≤ 0.7 Ω) should be used, and reserve a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR. Use three ceramic capacitors (10 pF, 33 pF and 100 nF) for composing the MLCC array, and place these

capacitors close to VBAT pins. The main power supply from an external application should be a single voltage source and can be expanded to two sub paths with the star topology structure. The width of VBAT trace should be not less than 2 mm respectively. As per design rules, the longer the VBAT trace is, the wider it should be.

In order to avoid the ripple and surge and ensure the stability of the power supply to the module, add a TVS diode with V_{RWM} = 4.7 V, low-clamp voltage and peak pulse current Ipp at the front end of the power supply.

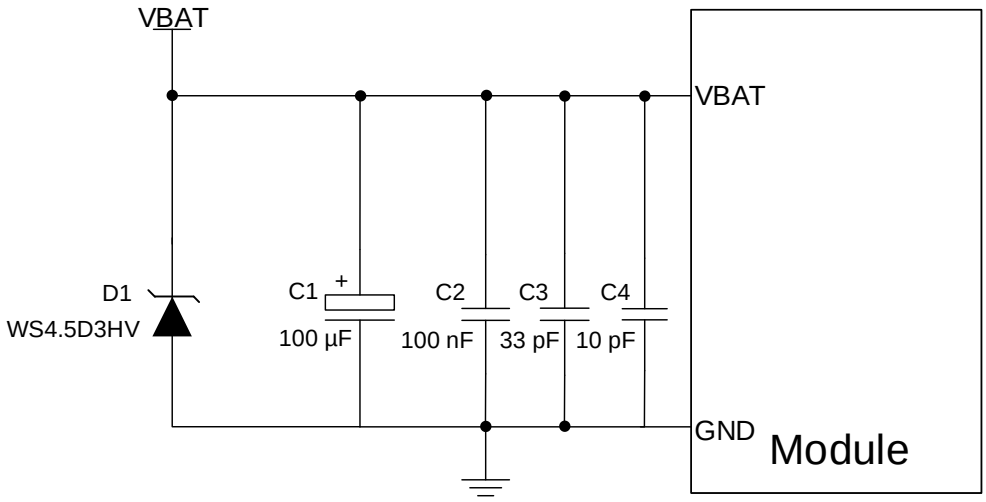


Figure 9: Reference Design of Power Supply

3.5. Turn-on

3.5.1. Turn-on with PWRKEY

Table 9: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	Pull down PWRKEY for at least 700 ms to turn on/off the module.

When the module is in power-down state, it can be turned on by driving PWRKEY low for at least 700 ms. It is recommended to use an open drain/collector driver to control PWRKEY.

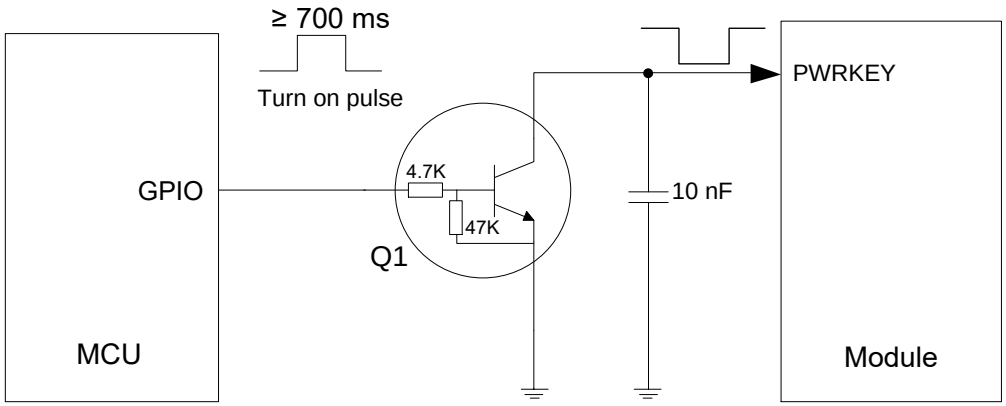


Figure 10: Reference Design of Turn-on with Driving Circuit

Another way to control PWRKEY is by using a push button directly. When pressing the button, an electrostatic strike may be generated from finger. Therefore, a TVS diode should be placed near the push button for ESD protection.

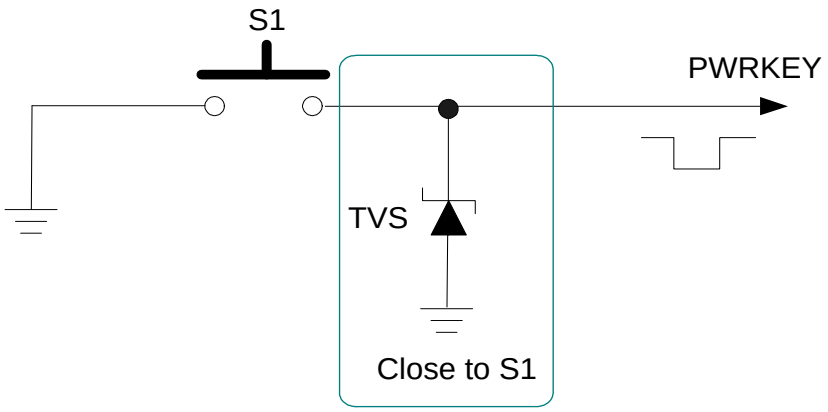


Figure 11: Reference Design of Turn-on with a Button

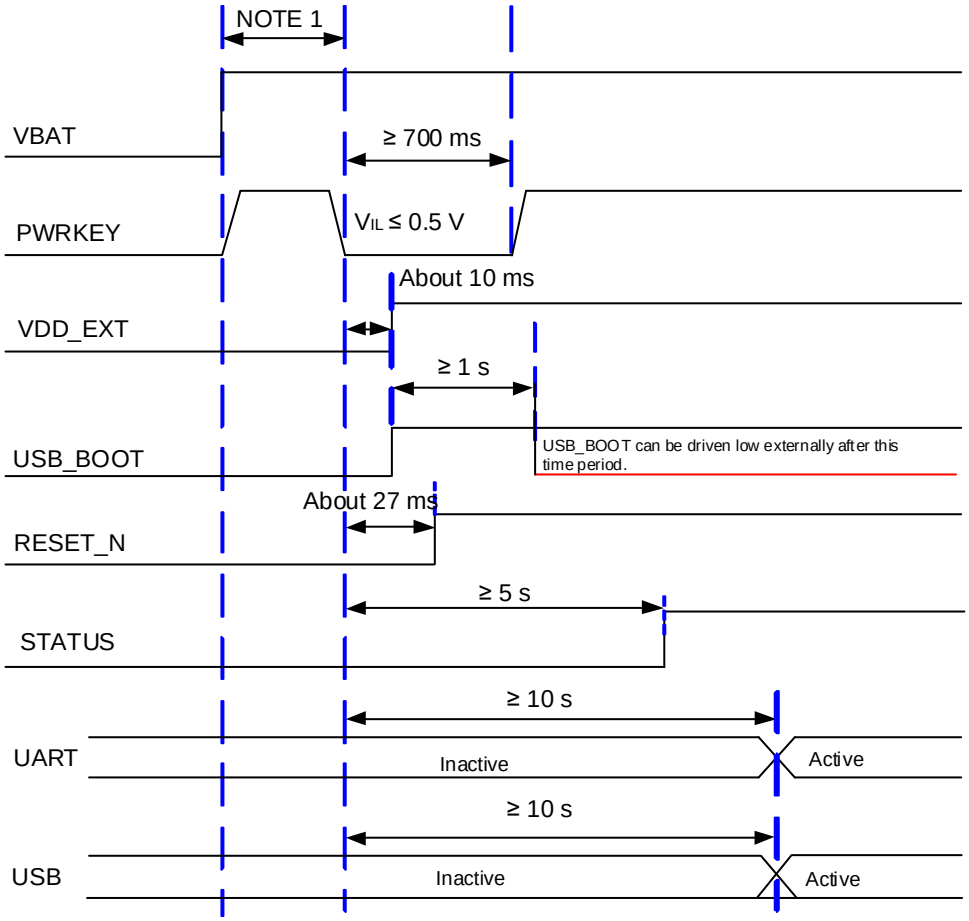


Figure 12: Timing Sequence of Turn-on with PWRKEY

NOTE

1. Ensure VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to be turned on automatically while power-off function is not needed, PWRKEY can be driven low directly to ground with a recommended 4.7 kΩ resistor.

3.6. Turn-off

3.6.1. Turn-off with PWRKEY

Drive PWRKEY low for at least 650 ms and then release it, the module will execute power-off procedure.

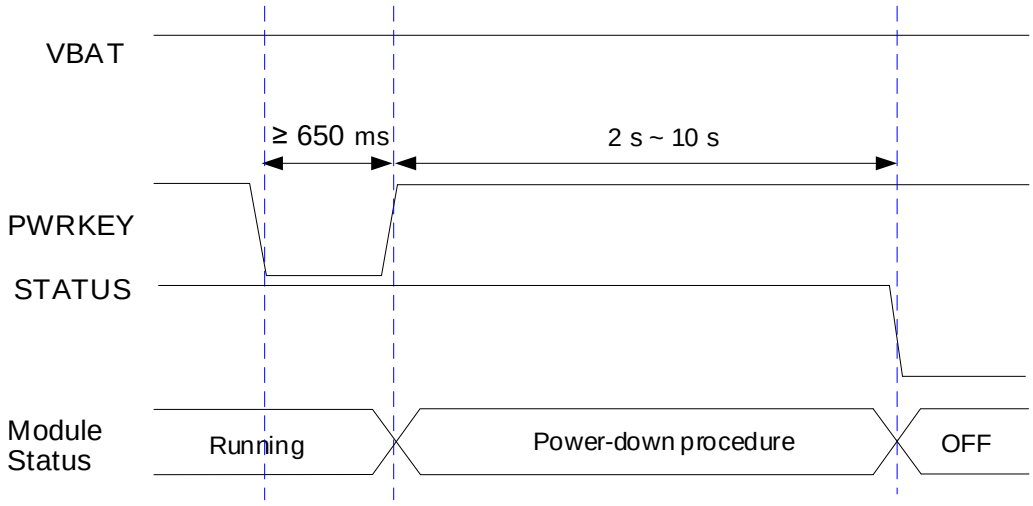


Figure 13: Timing Sequence of Turn-off with PWRKEY

3.6.2. Turn-off with AT Command

For proper shutdown procedure, execute **AT+QPOWD** which has similar timing and effect as turning off the module through driving PWRKEY low. See ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not cut off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command, can you cut off the power supply.
2. After executing the power off commands, keep the PWRKEY at high level, otherwise the module will be turned on again automatically after successful power-off.

3.7. Reset

Drive RESET_N low for at least 300 ms and then release it can reset the module. RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	15	DI	Reset the module	Active Low. If unused, keep it open.

The recommended circuit for reset function is similar to PWRKEY control circuit, you can use open drain/collector driver or button to control RESET_N.

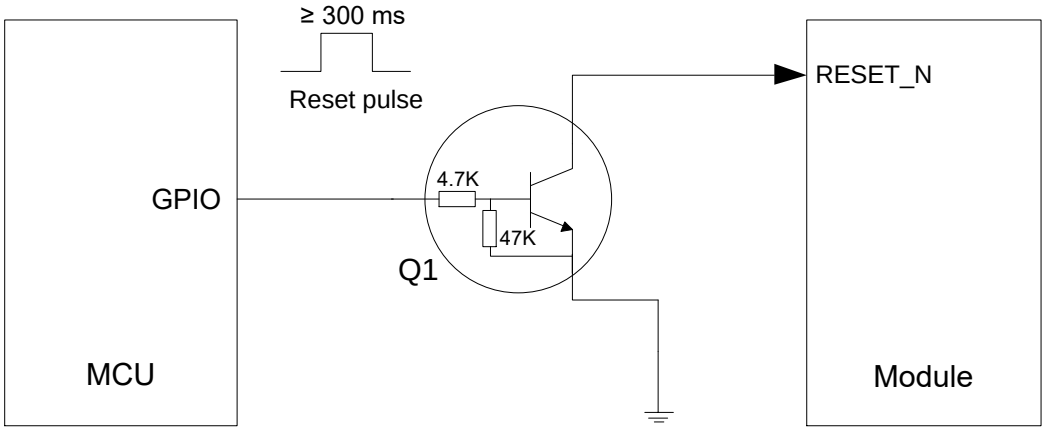


Figure 14: Reference Design of Reset with Driving Circuit

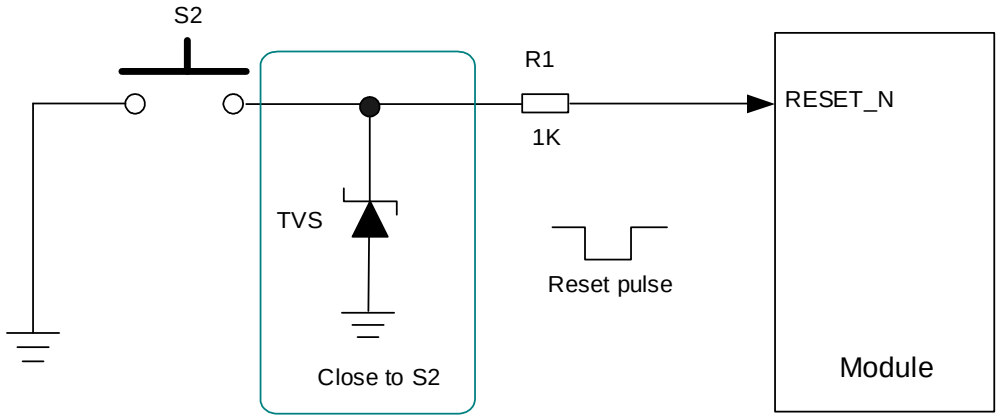


Figure 15: Reference Design of Reset with a Button

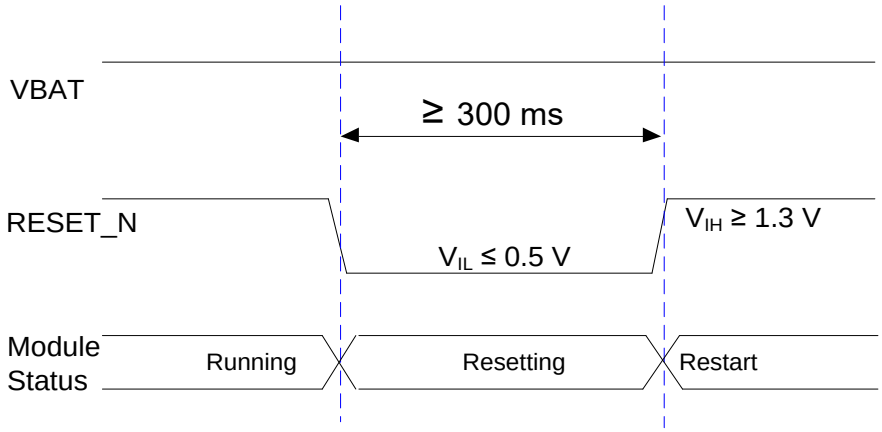


Figure 16: Timing Sequence of Reset

NOTE

1. Use RESET_N only when you fail to turn off the module with the **AT+QPOWD** and PWRKEY.
2. Make sure the capacitance on PWRKEY and RESET_N never exceeds 10 nF.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specifications and supports High-Speed (480 Mbps) and Full-Speed (12 Mbps) on USB 2.0. The USB interface can be used for AT command communication, data transmission, GNSS NMEA message output, software debugging and firmware upgrade.

Table 11: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	59	AIO	USB differential data (+)	USB 2.0 compliant. Require differential impedance of 90 Ω. If unused, keep them open.
USB_DM	60	AIO	USB differential data (-)	
USB_VBUS	61	AI	USB connection detect	If unused, keep it open.

It is recommended to use USB 2.0 interface for firmware upgrading and reserve test points for debugging.

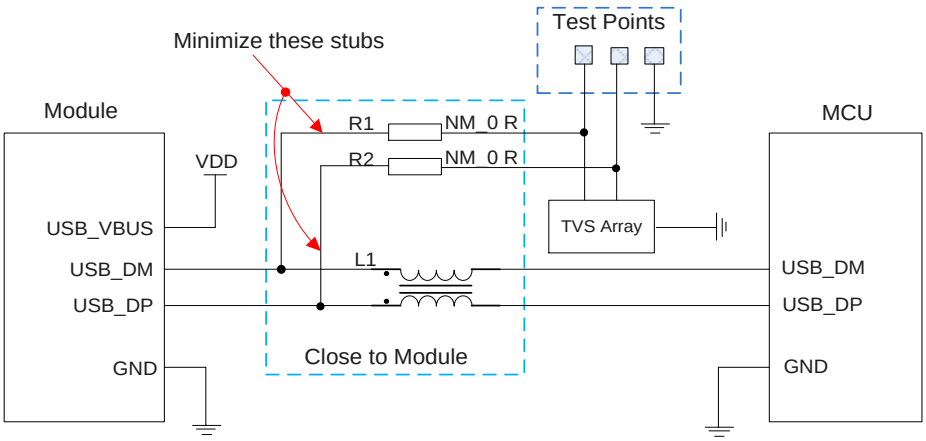


Figure 17: Reference Design of USB 2.0 Interface

It is recommended to add a common-mode choke L1 in series between MCU and the module to suppress EMI spurious transmission. Meanwhile, it is also suggested to add R1 and R2 in series between the module and test points for debugging. These resistors are not mounted by default. To ensure the signal integrity of USB 2.0 data transmission, L1, R1 and R2 should be placed close to the module, and resistors should be placed close to each other. Extra stubs of trace should be kept as short as possible.

To ensure performance, the following principles should be complied with when designing USB interface:

- The impedance of USB differential trace is 90 Ω. Route USB differential traces in the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Do not route signal traces under VBAT traces, crystal-oscillators, magnetic devices, sensitive circuits and provide clearance from RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Pay attention to the impact caused by junction capacitance of the ESD protection component on USB data traces. Typically, junction capacitance should be less than 2 pF.

For more details about the USB specifications, visit http://www.usb.org/home.

4.2. Emergency Download Interface

The module provides a USB_BOOT for emergency download. You can make the module enter emergency download mode by driving USB_BOOT low to GND before turning on the module. In this mode, the module supports firmware upgrade over USB 2.0 interface with shorter time period.

Table 12: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	82	DI	Force the module into emergency download mode	Active low. This pin cannot be pulled down to low level before the module starts up successfully if the emergency download mode is not necessary. It is recommended to reserve test points.

The following figure shows a reference design of USB_BOOT interface.

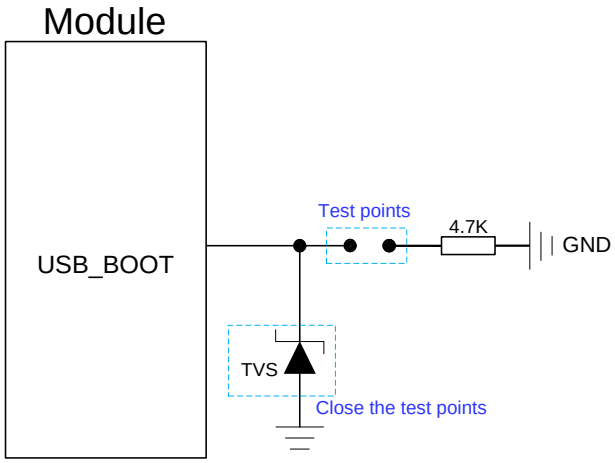


Figure 18: Reference Design of USB_BOOT

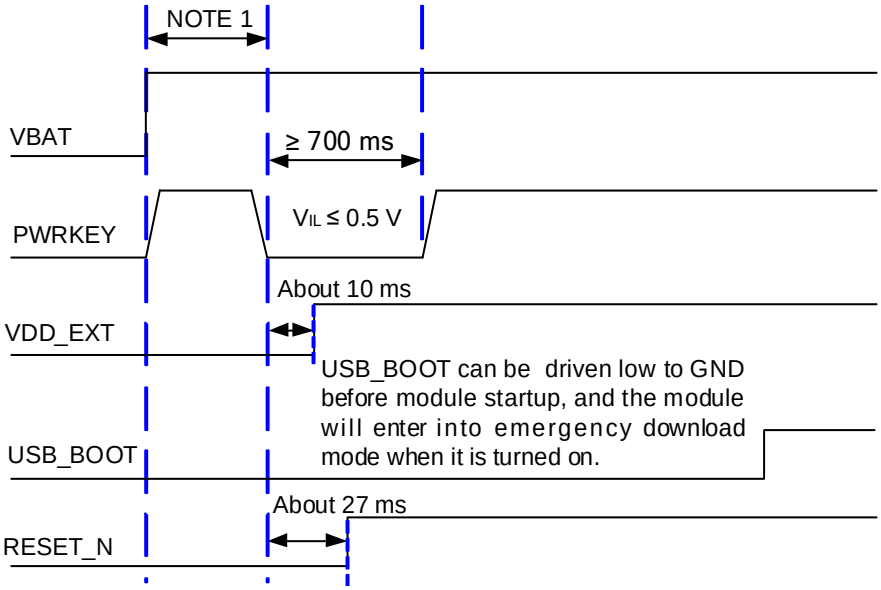


Figure 19: Timing Sequence of Entering Emergency Download Mode

NOTE

1. Ensure VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low shall be no less than 30 ms.
2. Follow the above timing sequence when using MCU to control module to enter the emergency download mode. Directly connect the test points as shown in ***Figure 18*** can manually force the module to enter emergency download mode.

3. Drive USB_BOOT low to GND and the pull-down resistor is recommended to be 4.7 kΩ.
4. The 6.0.1 and above version Qflash tool must be used for firmware upgrading.

4.3. USIM Interfaces

The USIM interfaces meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V USIM card is supported.

Table 13: Pin Description of USIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DATA	11	DIO	USIM1 card data	
USIM1_RST	12	DO	USIM1 card reset	
USIM1_CLK	13	DO	USIM1 card clock	
USIM1_VDD	14	PO	USIM1 card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM1_DET	79	DI	USIM1 card hot-swap detect	If unused, keep it open.
USIM2_VDD	65	PO	USIM2 card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM2_DATA	64	DIO	USIM2 card data	
USIM2_CLK	62	DO	USIM2 card clock	
USIM2_RST	63	DO	USIM2 card reset	

The module supports USIM card hot-swap via USIM_DET (level trigger pin), and both high and low level detections are supported. Hot-swap function is disabled by default, you can use **AT+QSIMDET** to configure this function. For details, see ***document [2]***.

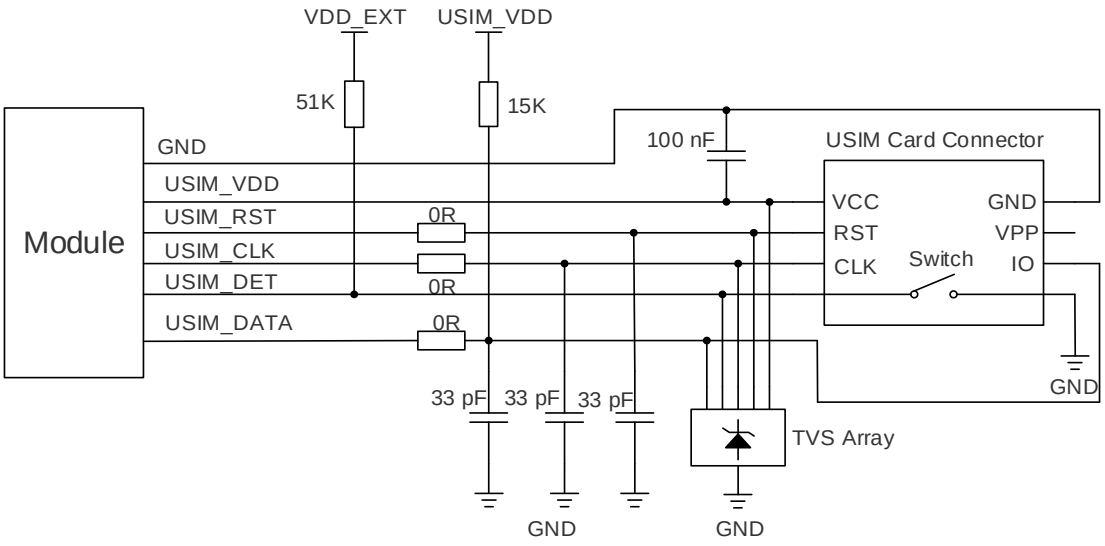


Figure 20: Reference Design of USIM Interface with an 8-pin USIM Card Connector

If the function of USIM card hot-swap is not needed, then keep USIM_DET floating.

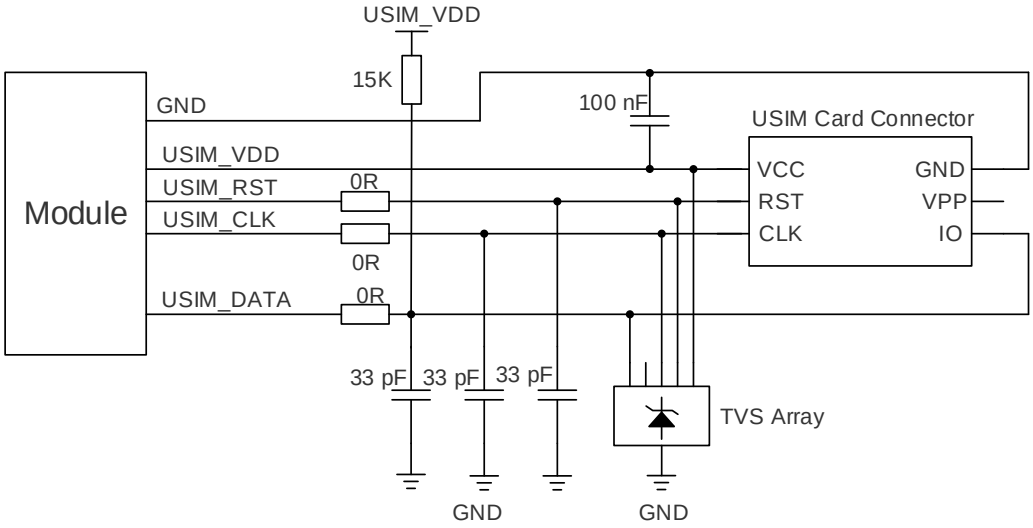


Figure 21: Reference Design of USIM Interface with a 6-pin USIM Card Connector

To enhance the reliability and availability of the USIM card in applications, follow the notes below for the USIM circuit design:

- Place USIM card connector close to the module. Keep the trace length less than 200 mm if possible.
- Keep USIM card signals away from RF and VBAT traces.
- Ensure the bypass capacitor between USIM_VDD and GND is less than 1 μF, and the capacitor should be placed close to the USIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.

- To offer better ESD protection, add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the USIM card to facilitate debugging. The 33 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST lines are used for filtering interference of EGSM900. Additionally, keep the USIM peripheral circuit close to the USIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the USIM card. If the USIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the USIM card connector.

NOTE

1. If GNSS function is selected, only USIM1 interface is supported. If GNSS is not selected, dual cards are supported.
2. Only USIM1 supports hot-swap function.

4.4. UART Interfaces

The module provides three UART interfaces:

Table 14: UART Interface Information

UART Types	Supported Baud Rates (bps)	Default Baud Rates (bps)	Functions
Main UART	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	Data transmission and AT command communication
Debug UART	115200	115200	Log output and GNSS NMEA message output
Auxiliary UART*	115200	115200	Communication with peripherals

Table 15: Pin Description of UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RXD	17	DI	Main UART receive	If unused, keep them open.
MAIN_TXD	18	DO	Main UART transmit	
MAIN_DTR	19	DI	Main UART data terminal ready	

MAIN_RI	20	DO	Main UART ring indication	
MAIN_DCD	21	DO	Main UART data carrier detect	
MAIN_CTS	22	DO	DTE clear to send signal from DCE	Connect to DTE's CTS. If unused, keep it open.
MAIN_RTS	23	DI	DTE request to send signal to DCE	Connect to DTE's RTS. If unused, keep it open.
AUX_RXD*	28	DI	Auxiliary UART receive	If unused, keep them open.
AUX_TXD*	29	DO	Auxiliary UART transmit	
DBG_RXD	38	DI	Debug UART receive	
DBG_TXD	39	DO	Debug UART transmit	

The module provides 1.8 V UART interfaces. You can use a voltage-level translator between the module and host's UART if the application is equipped with a 3.3 V UART. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design:

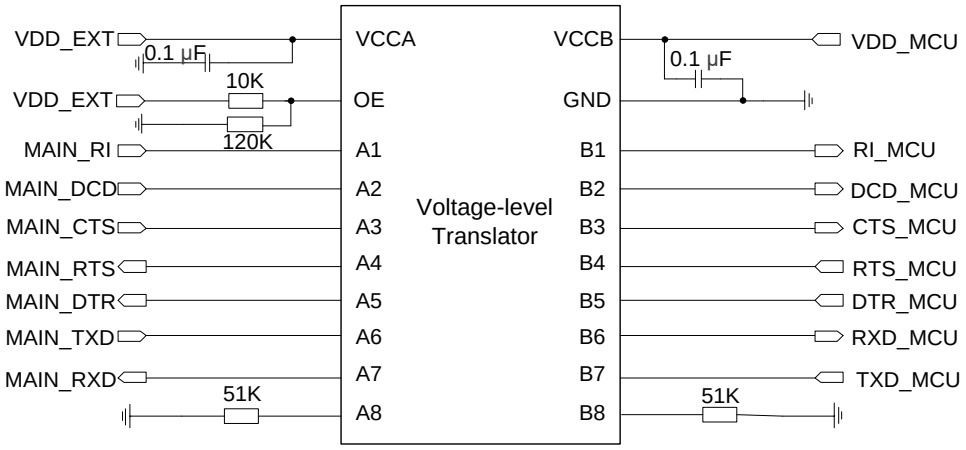


Figure 22: Reference Design of UART Interface with a Voltage-level Translator

Another example of level-shifting circuit is shown as below. Refer to the solid line for input/output circuit design in the dotted line below, but remember to follow the input/output sequence from or towards the module.

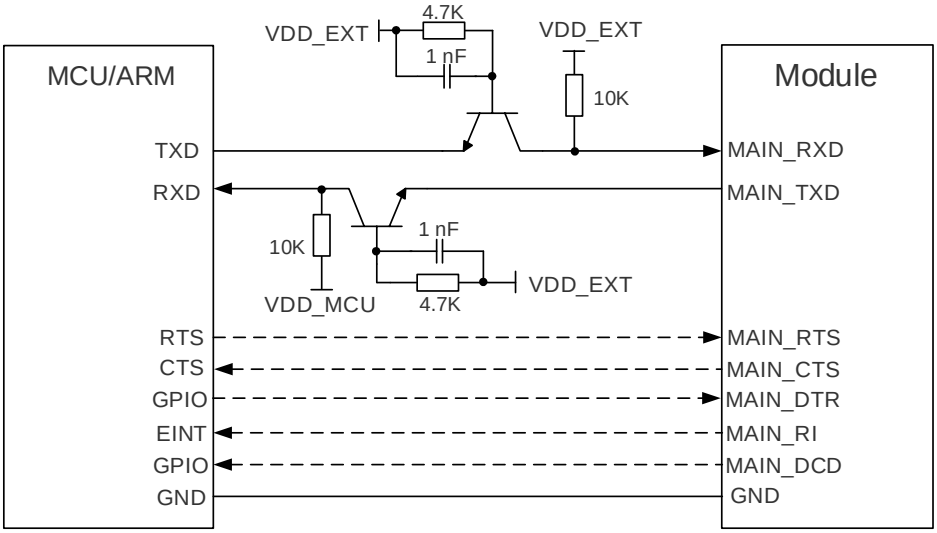


Figure 23: Reference Design of UART Interface with Triode Level-shifting Circuit

NOTE

1. Triode level-shifting circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS. Please also pay attention to the direction of connection.

4.5. I2C Interface

The module provides one I2C interface:

Table 16: Pin Description of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SDA	66	OD	I2C serial data	An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SCL	67	OD	I2C serial clock	

4.6. PCM Interface

The module provides one PCM interface:

Table 17: Pin Description of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK	30	DO	PCM clock	1.8 V power domain. If unused, keep them open.
PCM_SYNC	31	DO	PCM data frame sync	
PCM_DIN	32	DI	PCM data input	
PCM_DOUT	33	DO	PCM data output	

The PCM interface supports primary mode (short frame synchronization), the module only works as a master device.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK.

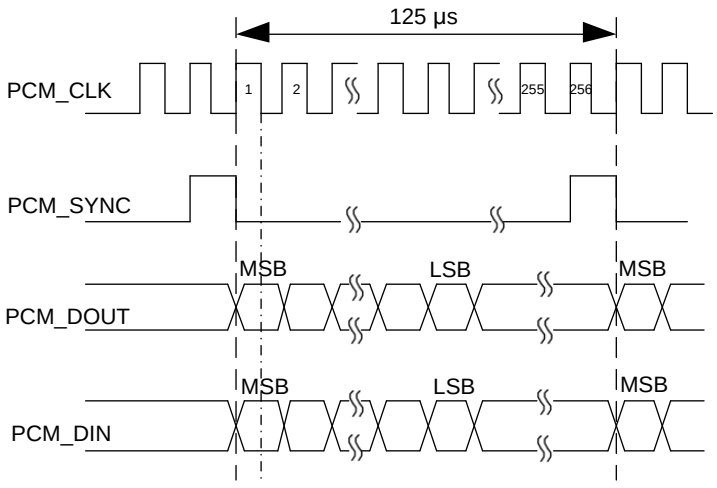


Figure 24: Timing Sequence of Primary Mode

In short frame mode, data is sampled on the falling edge of PCM_CLK, and sent on the rising edge. The falling edge of PCM_SYNC represents the high effective bit. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz, and 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

Clock and mode of PCM can be configured by AT command, and the default configuration is master mode using short frame sync format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. For details, see ***document [3]*** about **AT+QDAI**.

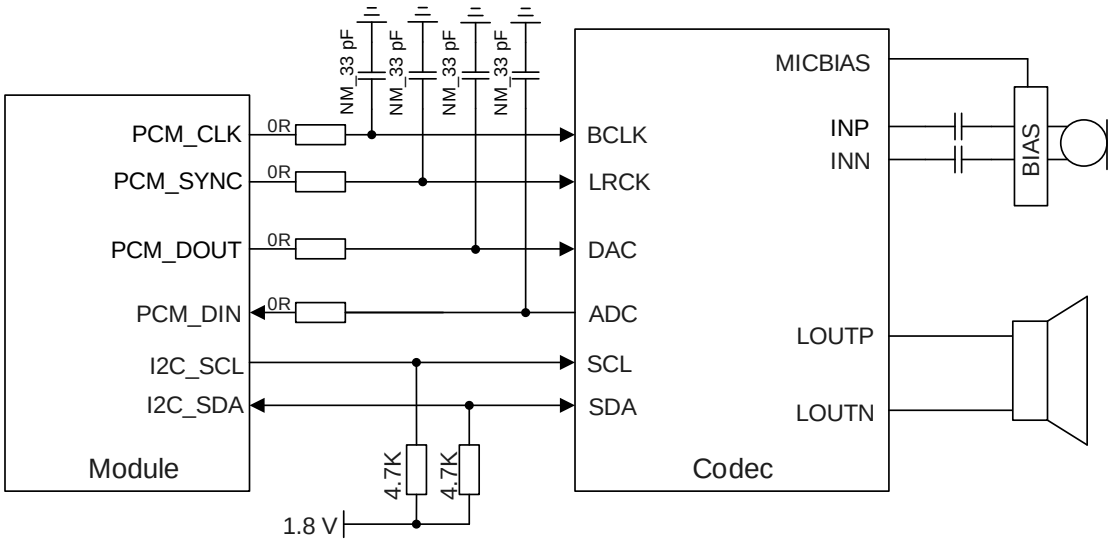


Figure 25: Reference Design of PCM Interface and I2C Interface

NOTE

1. PCM and I2C function are both optional. If those interfaces are not used, keep them floated.
2. It is recommended to reserve an RC (R = 0 Ω, C = 33 pF) circuit on the PCM traces, especially for PCM_CLK.
3. The module can only be used as a master device in applications related to PCM and I2C interfaces.

4.7. Analog Audio Interfaces

The module provides one analog input channel and one analog output channel.

Table 18: Pin Description of Analog Audio Interface

Pin Name	Pin No.	I/O	Description	Comment
MIC_P	3	AI	Microphone analog input (+)	If unused, keep them open.
MIC_N	4	AI	Microphone analog input (-)	

SPK_P	5	AO	Analog audio differential output (+)	Used for earpiece. The interface can drive 32 Ω earpiece with power rate at 37 mW. It can also be used to drive external power amplifier devices if the output power rate cannot meet the demand. If unused, keep them open.
SPK_N	6	AO	Analog audio differential output (-)	

- AIN channels are differential input channels which can be applied for input from microphone (usually an electret microphone is used).
- AOUT channels are differential output channels which can be applied for output through loudspeaker and earpiece.
- The module's internal audio amplifier is configured as Class AB by default.

NOTE

1. The analog audio function is optional. If those interfaces are not used, keep them floated.
2. If analog audio function is selected and GNSS function is also needed, the analog audio input interface requires an external microphone bias circuit. MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO. When GNSS function is not needed, the analog audio input interface requires no external microphone bias circuit.

4.7.1. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g. 10 pF and 33 pF) to filter out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied to filter out RF interference when the module is transmitting at EGSM900. Without this capacitor, TDD noise could be heard during the call. The 10 pF capacitor here is used to filter out RF interference at DCS1800. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you need to discuss with your capacitor vendors to choose the most suitable capacitor to filter out high-frequency noises at EGSM900/DCS1800.

The severity degree of the RF interference in the voice channel during GSM transmitting largely depends on the application design. In some cases, EGSM900 TDD noise is more severe; while in other cases, DCS1800 TDD noise is more obvious. Therefore, a suitable capacitor can be selected based on the test results. The filter capacitor on the PCB should be placed as close as possible to the audio device or audio interface, and the trace should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease radio or other signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.7.2. Microphone Interface Reference Design

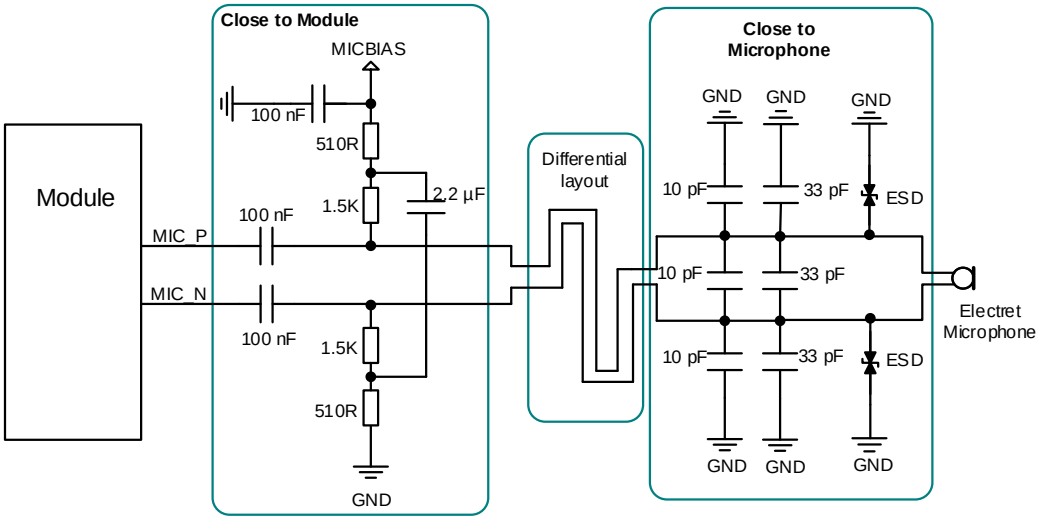


Figure 26: Reference Design with MICBIAS of Microphone Interface

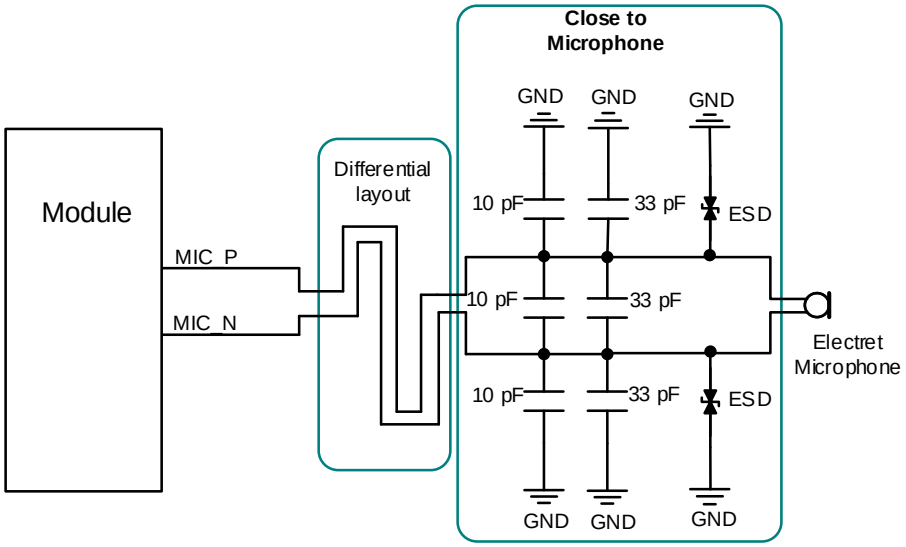


Figure 27: Reference Design Without MICBIAS of Microphone Interface

NOTE

1. MIC channel is sensitive to ESD, so do not remove the ESD protection components used to protect the MIC.
2. When the analog audio input function is needed:
   - The module requires an external microphone bias circuit if GNSS function is selected. And MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO. See ***Figure 26*** for microphone interface circuit design.
   - The module requires no external microphone bias circuit if GNSS function is not selected, see ***Figure 27*** for microphone interface circuit design.

4.7.3. Earpiece Interface Reference Design

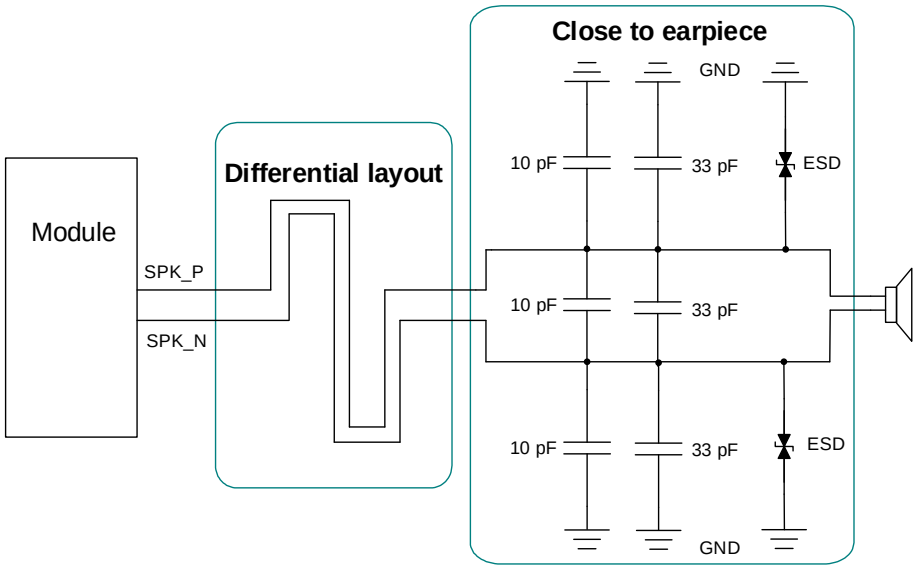


Figure 28: Reference Design of Earpiece Interface

4.7.4. Loudspeaker Interface Reference Design

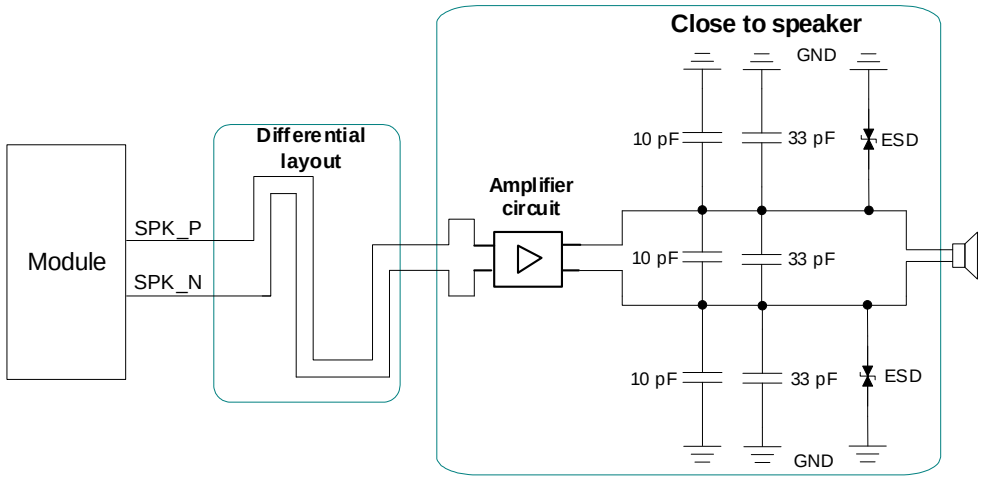


Figure 29: Reference Design of Loudspeaker Interface

For differential input and output audio power amplifiers, please visit http://www.ti.com/ to obtain the required devices. There are also many audio power amplifiers with the same performance to choose from on the market.

4.8. ADC Interfaces

The module provides two ADC interfaces. To improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

Table 19: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	9	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	96	AI		

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1

For more details about the AT command, see ***document [2]***.

Table 20: Characteristics of ADC Interface

Parameters	Min.	Typ.	Max.	Units
ADC0 voltage range	0	-	1.2	V
ADC1 voltage range	0	-	1.2	V
ADC resolution	-	-	12	bits

NOTE

1. A voltage divider with resistance of more than 100 kΩ must be used for ADC interface application.
2. The accuracy of the two resistors in each voltage divider affects the sampling error of the ADC. It is recommended to use resistors with an accuracy of 1%; if the accuracy of the ADC needs to be higher, resistors with an accuracy of 0.5% are recommended. See ***document [4]*** for details.

4.9. Indication Signal

Table 21: Pin Description of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	16	DO	Indicate the module's network activity status	If unused, keep them open.
STATUS	25	DO	Indicate the module's operation status	

4.9.1. Network Status Indication

The module provides one network status indication pin: NET_STATUS for module's network registration status indication. This pin can be used to drive corresponding LED.

Table 22: Network Status Indication Pin Level Status and Module Network Status

Pin Name	Level Status	Module Network Status
NET_STATUS	Flicker slowly (200 ms high level/1800 ms low level)	Network searching
	Flicker slowly (1800 ms high/200 ms low level)	Idle
	Flicker quickly (125 ms high level /125 ms low level)	Data transmission is ongoing

High level	Voice calling

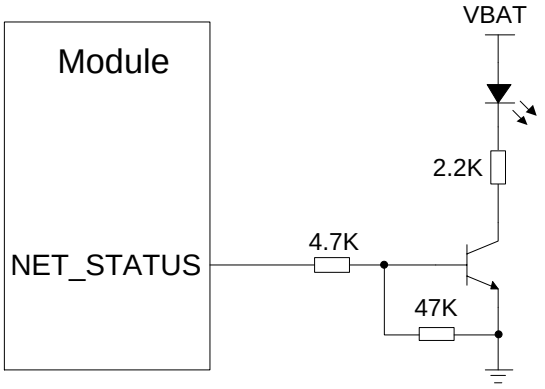


Figure 30: Reference Design of Network Status Indication

4.9.2. STATUS

STATUS indicates the module's operation status. It will output high level when module is turned on successfully.

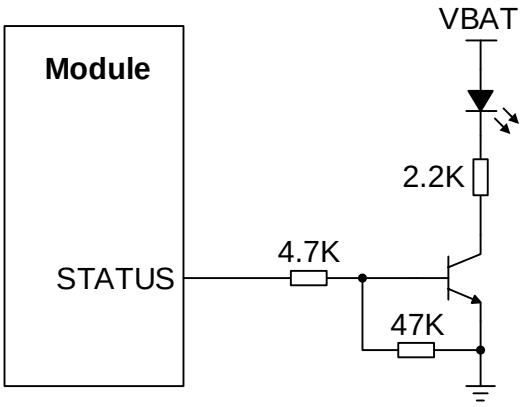


Figure 31: Reference Design of STATUS

4.9.3. MAIN_RI

AT+QCFG= "risignaltype", "physical" can be used to configure the indication behavior for MAIN_RI. No matter on which port (main UART, USB AT port or USB modem port) a URC is presented, the URC will trigger the behavior of MAIN_RI.

NOTE

The **AT+QURCCFG** allows you to set main UART, USB AT port or USB modem port as the URC output port. The USB AT port is used to send AT commands by default.

MAIN_RI behaviors can be configured flexibly, and default behaviors are shown as below:

Table 23: MAIN_RI Level Status and Module Status

Module Status	MAIN_RI Level Status
Idle	High level
When a new URC return	MAIN_RI outputs at least 120 ms low level. After the module outputs the data, the level status will then become high.

Indication behavior of MAIN_RI can be configured via several commands, e.g. **AT+QCFG="urc/ri/ring"** can be used to specify the MAIN_RI behavior when the URC indicating an incoming call is reported. See ***document [2]*** for details.

5 RF Specifications

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

Table 24: Pin Description of Cellular Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	35	AIO	Main antenna interface	50 Ω impedance.

NOTE

The module supports Wi-Fi Scan function. As this function shares the same antenna with main antenna interface, then both functions cannot be used at the same time. Wi-Fi scan only supports receiving function.

Table 25: Operating Frequency (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B5	824–849	869–894
LTE-FDD B8	880–915	925–960
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400

LTE-TDD B41	2535–2675	2535–2675

NOTE

Band 41 only supports 140 MHz (2535–2675 MHz).

5.1.2. Tx Power

Table 26: RF Transmitting Power

Frequency	Max.	Min.
LTE-FDD B1/B3/B5/B8	23 dBm ±2 dB	< -39 dBm
LTE-TDD B34/B38/B39/B40/B41	23 dBm ±2 dB	< -39 dBm

5.1.3. Rx Sensitivity

Table 27: Conducted RF Receiving Sensitivity

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO	
LTE-FDD B1 (10 MHz)	-99.5 dBm	-	-	-96.3 dBm
LTE-FDD B3 (10 MHz)	-99.0 dBm	-	-	-93.3 dBm
LTE-FDD B5 (10 MHz)	-98.5 dBm	-	-	-94.3 dBm
LTE-FDD B8 (10 MHz)	-99.0 dBm	-	-	-93.3 dBm
LTE-TDD B34 (10 MHz)	-100.0 dBm	-	-	-96.3 dBm
LTE-TDD B38 (10 MHz)	-99.0 dBm	-	-	-96.3 dBm
LTE-TDD B39 (10 MHz)	-100.0 dBm	-	-	-96.3 dBm
LTE-TDD B40 (10 MHz)	-100.5 dBm	-	-	-96.3 dBm
LTE-TDD B41 (10 MHz)	-99.0 dBm	-	-	-94.3 dBm

5.1.4. Reference Design

Use a π-type matching circuit for all the antenna interfaces for better cellular performance. Capacitors are not mounted by default.

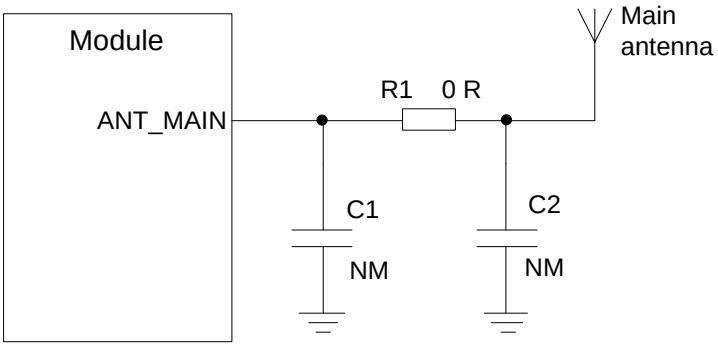


Figure 32: Reference Design of Main Antenna and Diversity Antenna

NOTE

1. To reduce the coexistence problems and avoid the interference of receiving sensitivity, make sure that the isolation between antennas is no less than 20 dB.
2. Place the π-type matching components (R1, C1, C2) as close to antennas as possible.

5.2. GNSS

GNSS function is optional for the module. The information is as follows:

- The module supports GPS, BDS, GLONASS and Galileo positioning system.
- The module supports NMEA 0183 protocol and does not output NMEA message by default. NMEA message can be output by USB interface or debugging UART interface via AT command (update rate for positioning: 1 Hz).
- The module's GNSS function is switched off by default. It must be switched on via AT command.

For more details about AT commands, see ***document [5]***.

5.2.1. Antenna Interface & Frequency Bands

Table 28: GNSS Frequency (Unit: MHz)

Antenna Type	Frequency
GPS	1575.42 ±1.023 (L1)
BDS	1561.098 ±2.046 (B1I)
Galileo	1575.42 ±2.046 (E1)
GLONASS	1597.5–1605.8 (L1)

5.2.2. GNSS Performance

Table 29: GNSS Performance

Parameters	Descriptions	Typ.	Unit
Sensitivity	Acquisition	-146	dBm
	Reacquisition	-160	
	Tracking	-160	
TTFF	Cold start @ open sky	28	s
	Warm start @ open sky	27	
	Hot start @ open sky	3.7 [3]	
Accuracy	CEP-50	2	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock of navigation signals (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

[3] The time of sending firmware package is contained.

5.2.3. GNSS Antenna Reference Design

5.2.3.1. GNSS Active Antenna

GNSS active antenna connection reference circuit is shown in the figure below.

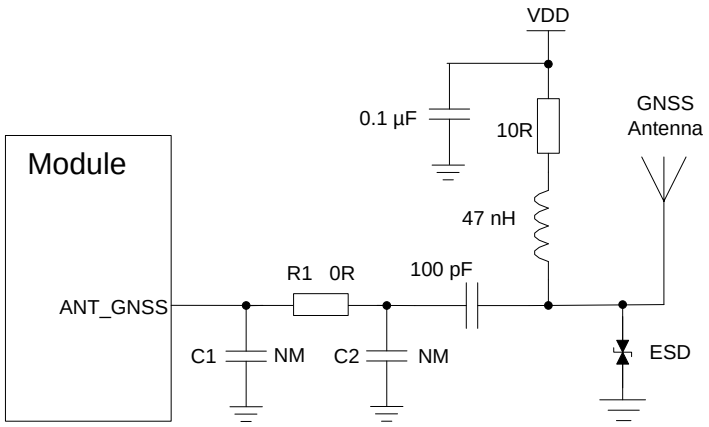


Figure 33: Reference Design of GNSS Active Antenna

The power supply voltage range of the external active antenna is 2.8–4.3 V, and the typical value is 3.3 V.

5.2.3.2. GNSS Passive Antenna

GNSS passive antenna connection reference circuit is shown in the figure below.

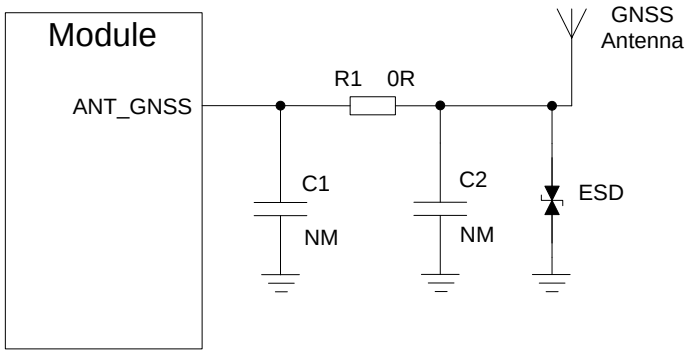


Figure 34: Reference Design of GNSS Passive Antenna

C1, R1 and C2 form the matching circuit, which is recommended to be reserved for adjusting the antenna impedance. Among them, C1 and C2 are not mounted by default, and R1 is only mounted by a 0 Ω resistor. The impedance of the RF trace should be controlled at about 50 Ω, and the trace should be

as short as possible.

NOTE

1. The external LDO can be selected according to the active antenna requirements. If the module is designed with a passive antenna, then the VDD circuit is not needed.
2. Junction capacitance of ESD protection components on the antenna interface should not exceed 0.05 pF.
3. GNSS function of the module is optional.
   - If both GNSS and analog audio input function are selected, the module requires an external microphone bias circuit. And MICBIAS must be provided with 1.8 V power supply by using a low-noise LDO. Only USIM1 interface is supported on this condition.
   - If GNSS function is not selected but analog audio input function is needed, the module requires no external microphone bias circuit. And dual USIM cards are supported in this situation.

5.3. Reference Design of RF Routing

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

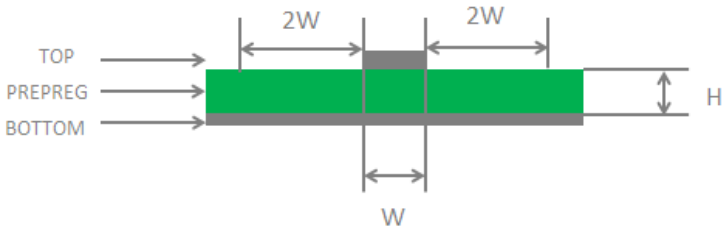


Figure 35: Microstrip Design on a 2-layer PCB

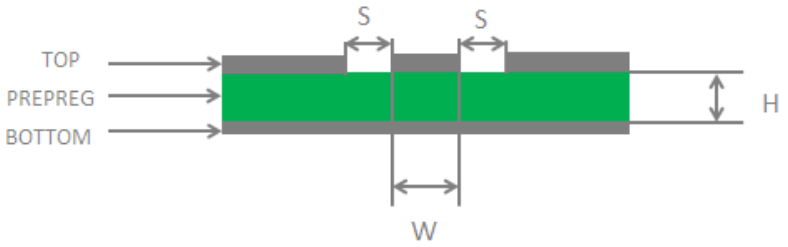


Figure 36: Coplanar Waveguide Design on a 2-layer PCB

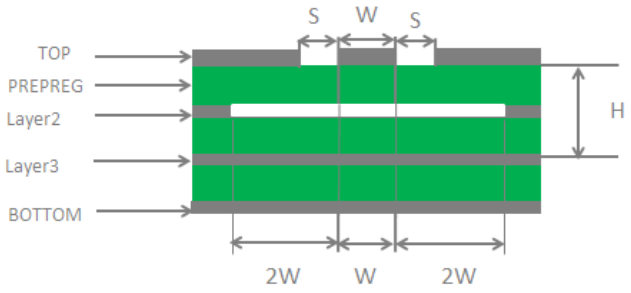


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

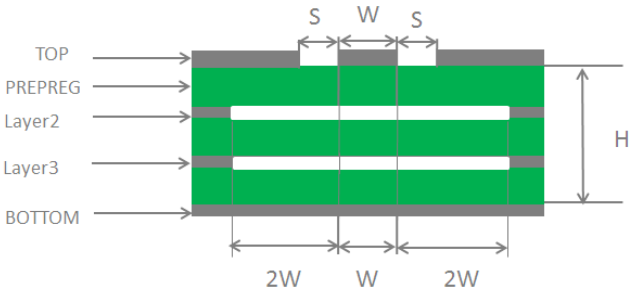


Figure 38: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance

between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).

- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [6]***.

5.4. Requirements for Antenna Design

Table 30: Requirements for Antenna Design

Antenna Types	Requirements
GNSS	● Frequency range: L1: 1559–1609 MHz ● VSWR: < 2 (Typ.) ● Passive antenna gain: > 0 dBi ● Active antenna noise figure: < 1.5 dB ● Active antenna gain: > -2 dBi ● Active antenna embedded LNA gain: < 17 dB
LTE	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

5.5. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connectors provided by Hirose.

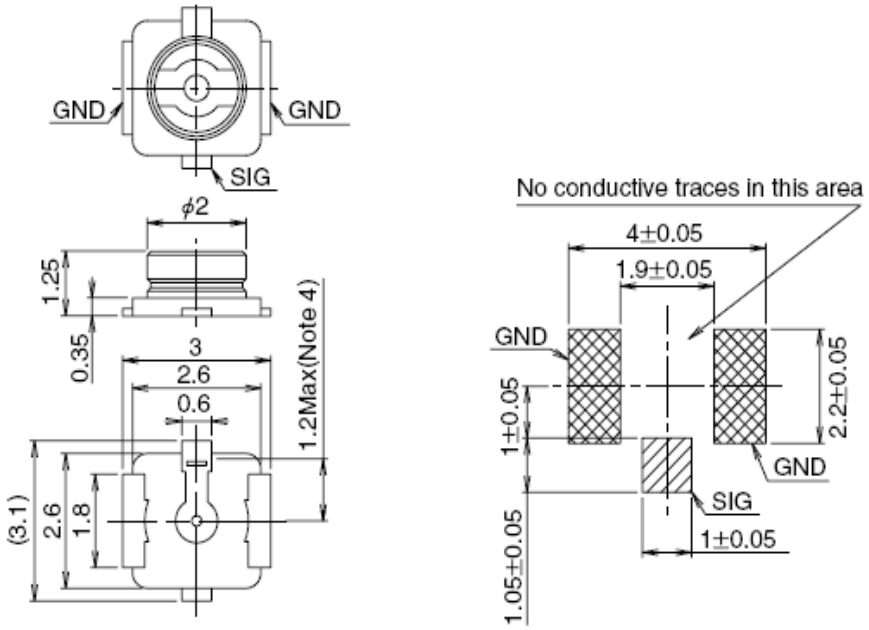


Figure 39: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

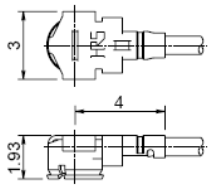
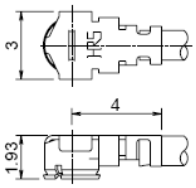
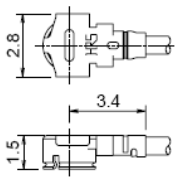
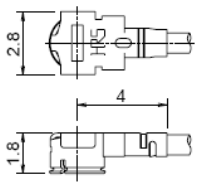
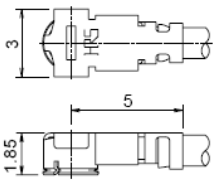
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 40: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connectors.

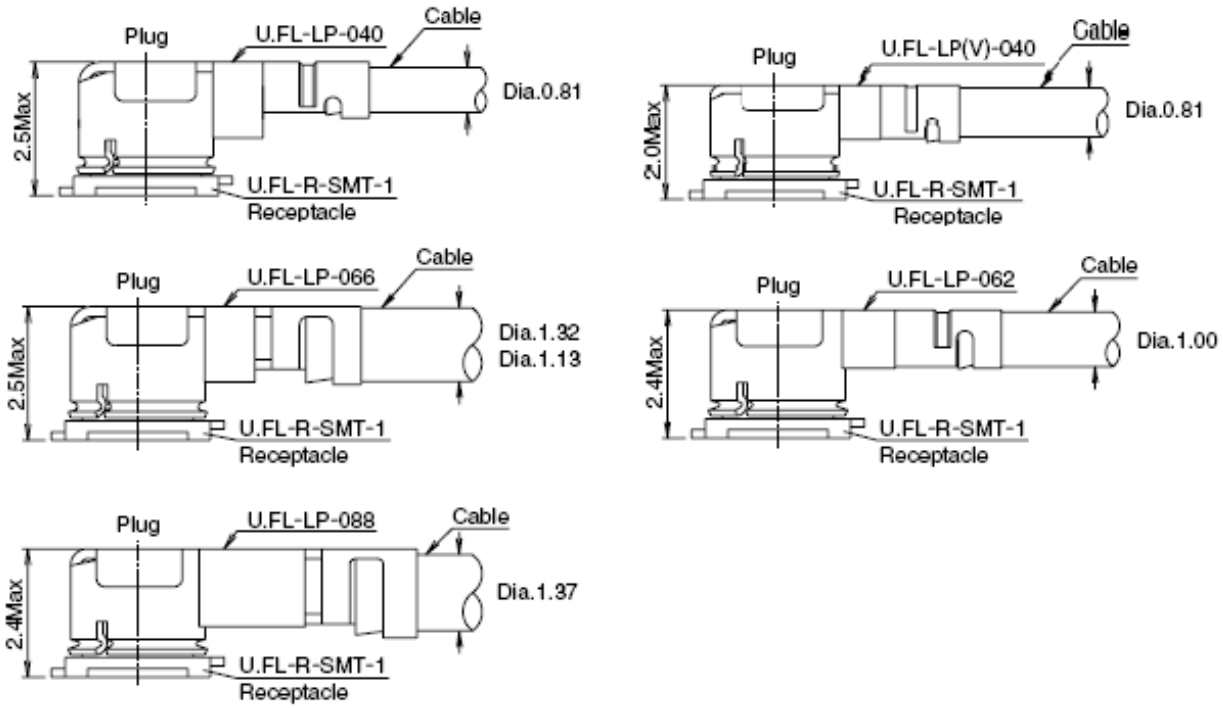


Figure 41: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Table 31: Absolute Maximum Ratings

Parameters	Min.	Max.	Unit
Voltage at VBAT	-0.3	6	V
Voltage at USB_VBUS	-0.3	5.5	V
Voltage at digital pins	-0.3	2.3	V
Voltage at ADC0	-	1.2	V
Voltage at ADC1	-	1.2	V
Current at VBAT	-	2	A

6.2. Power Supply Ratings

Table 32: Module Power Supply Ratings

Parameters	Descriptions	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltage must be within this range	3.4	3.8	4.3	V
	Voltage drops during transmitting burst	Maximum power control level at LTE	-	-	400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at LTE	-	1.5	2	A

USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V

6.3. Power Consumption

Table 33: Power Consumption

Modes	Conditions	Typ.	Units
OFF state	Power down	38	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.8	mA
	AT+CFUN=4 (USB disconnected)	0.92	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.74	mA
	LTE-FDD @ PF = 64 (USB disconnected)	1.37	mA
	LTE-FDD @ PF = 64 (USB suspend)	1.51	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.13	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.03	mA
	LTE-TDD @ PF = 32 (USB disconnected)	1.75	mA
	LTE-TDD @ PF = 64 (USB disconnected)	1.34	mA
	LTE-TDD @ PF = 64 (USB suspend)	1.49	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.14	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.03	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	16.72	mA
	LTE-FDD @ PF = 64 (USB connected)	29.46	mA
	LTE-TDD @ PF = 64 (USB disconnected)	16.72	mA
	LTE-TDD @ PF = 64 (USB connected)	29.43	mA
LTE data transmission	LTE-FDD B1	537	mA
	LTE-FDD B3	510	mA

	LTE-FDD B5	515	mA
	LTE-FDD B8	490	mA
	LTE-TDD B34	200	mA
	LTE-TDD B38	180	mA
	LTE-TDD B39	186	mA
	LTE-TDD B40	180	mA
	LTE-TDD B41	185	mA

6.4. Digital I/O Characteristics

Table 34: 1.8 V I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	Input high voltage	0.7 × VDDIO	VDDIO + 0.2
V_{IL}	Input low voltage	-0.3	0.3 × VDDIO
V_{OH}	Output high voltage	VDDIO – 0.2	-
V_{OL}	Output low voltage	-	0.2

Table 35: USIM 1.8 V I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
USIM_VDD	Power supply	1.62	1.98
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD
V_{IL}	Input low voltage	0	0.2 × USIM_VDD
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD
V_{OL}	Output low voltage	0	0.15 × USIM_VDD

Table 36: USIM 3.0 V I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
USIM_VDD	Power supply	2.7	3.3
V_{IH}	Input high voltage	0.7 × USIM_VDD	USIM_VDD
V_{IL}	Input low voltage	0	0.15 × USIM_VDD
V_{OH}	Output high voltage	0.7 × USIM_VDD	USIM_VDD
V_{OL}	Output low voltage	0	0.15 × USIM_VDD

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 37: ESD Characteristics (Temperature: 25 °C, Humidity: 45 %; Unit: kV)

Test Points	Contact Discharge	Air Discharge
VBAT & GND	±5	±10
All antenna interfaces	±4	±8
Other interfaces	±0.5	±1

6.6. Operating and Storage Temperatures

Table 38: Operating and Storage Temperatures (Unit: °C)

Parameters	Min.	Typ.	Max.
Normal Operating Temperature [4]	-35	+25	+75
Extended Operating Temperature [5]	-40	-	+85
Storage Temperature	-40	-	+90

[4] Within this range, the module can meet 3GPP specifications.
[5] Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call*, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

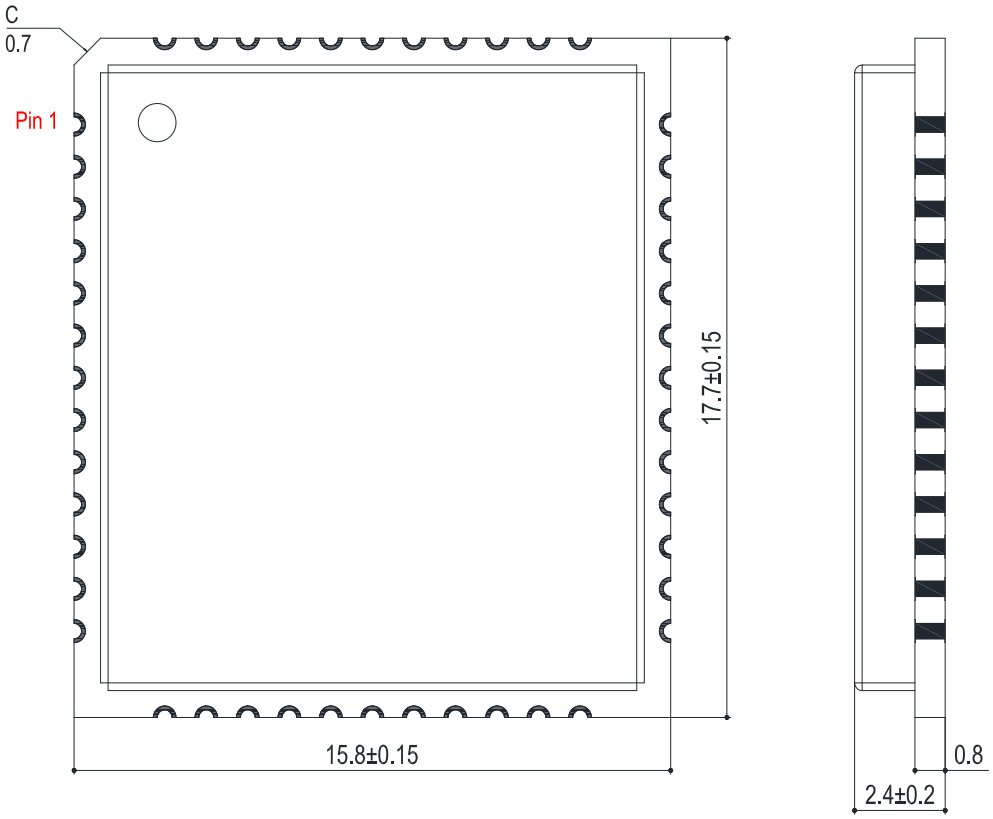


Figure 42: Module Top and Side Dimensions

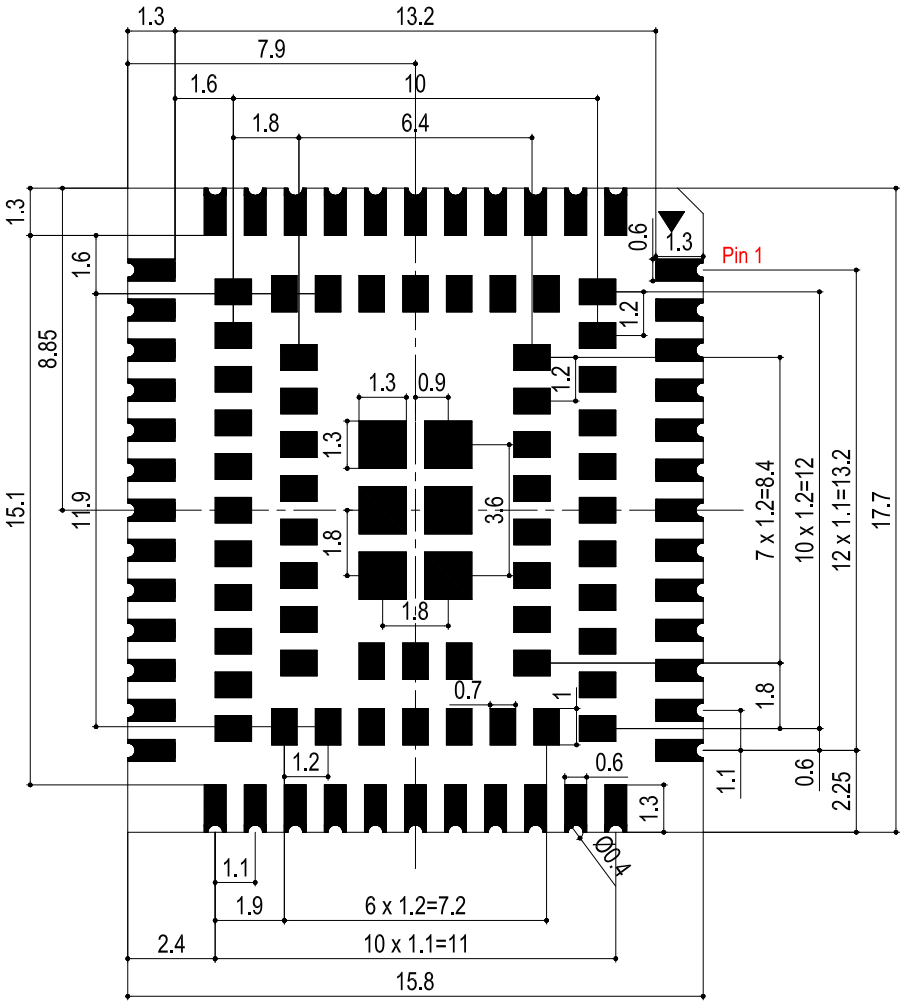


Figure 43: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

7.2. Recommended Footprint

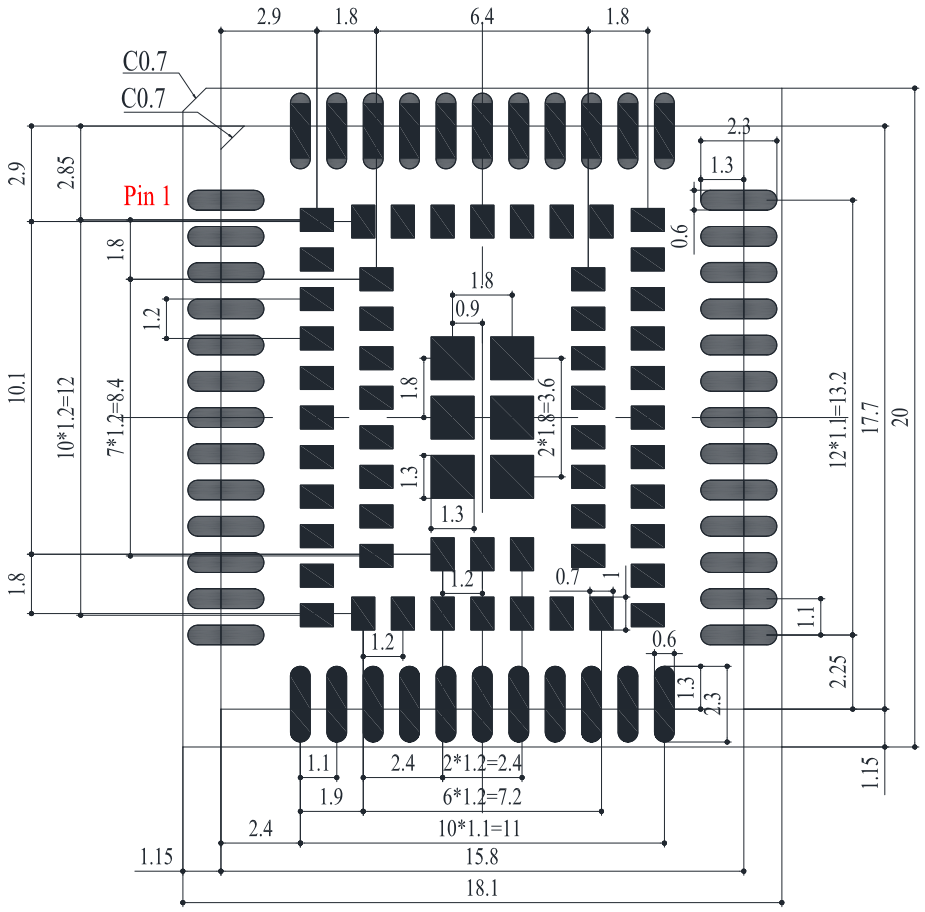


Figure 44: Recommended Footprint (Top View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

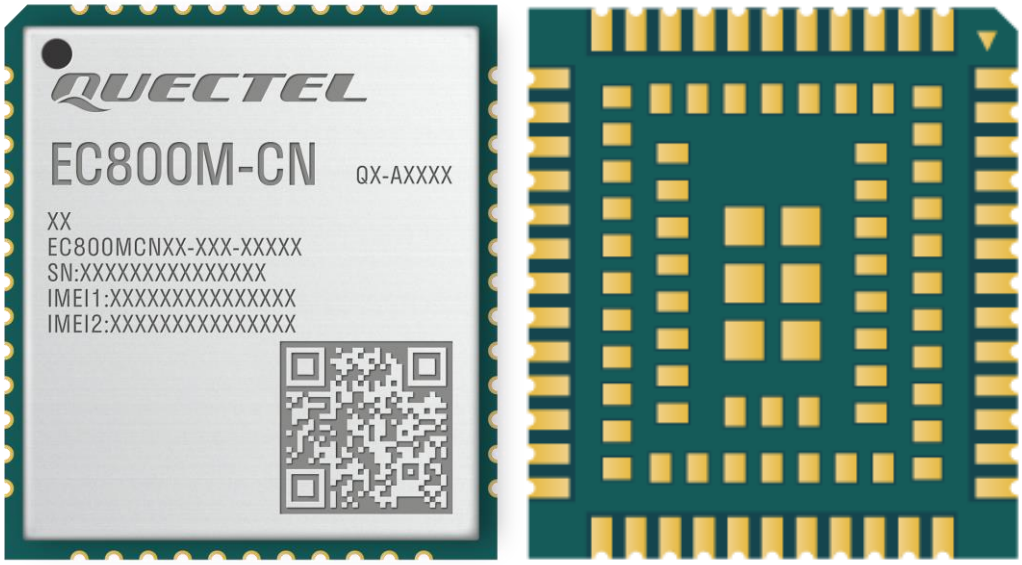


Figure 45: Top View and Bottom View of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [6] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[6] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20 mm. For more details, see ***document [7]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

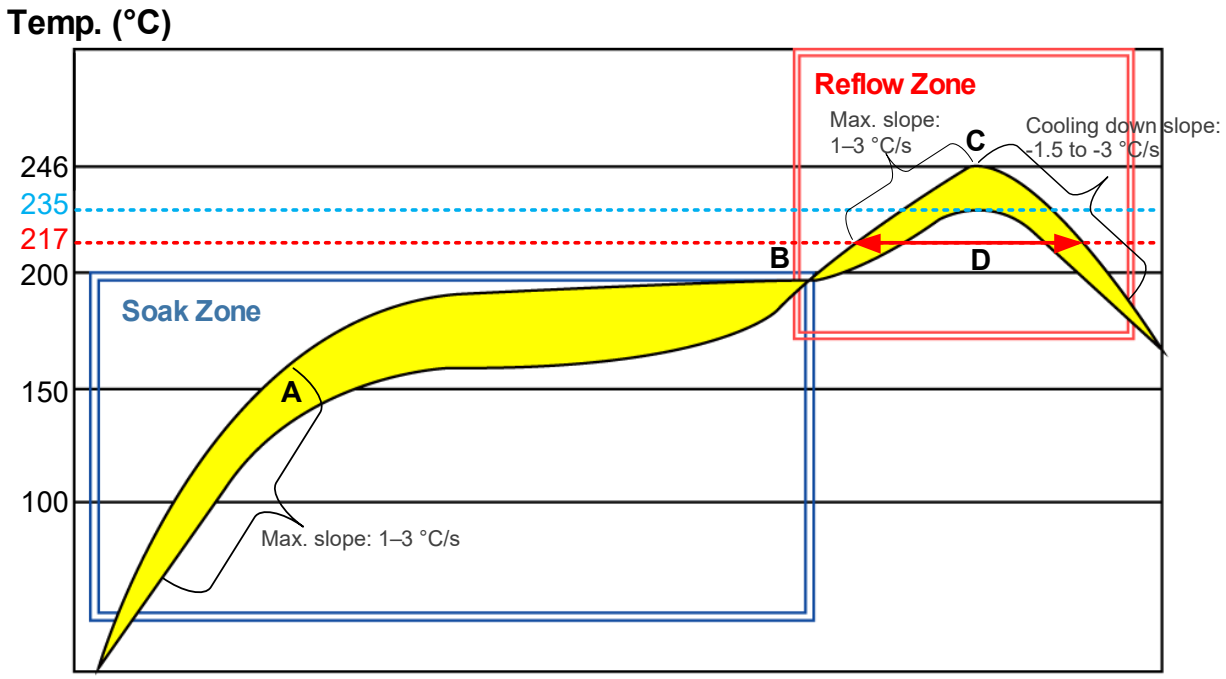


Figure 46: Recommended Reflow Soldering Thermal Profile

Table 39: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [7]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

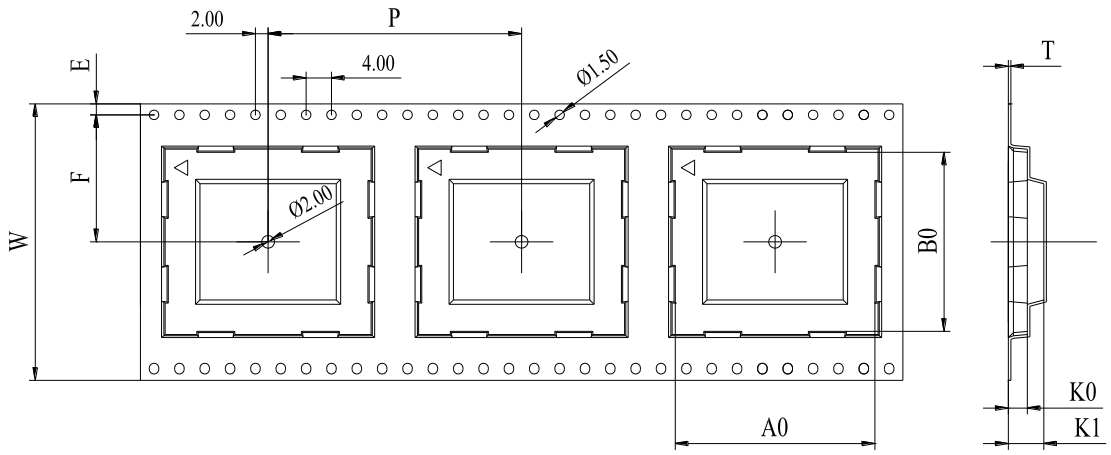


Figure 47: Carrier Tape Dimension Drawing

Table 40: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	24	0.4	16.2	18.1	2.8	7.6	14.2	1.75

8.3.2. Plastic Reel

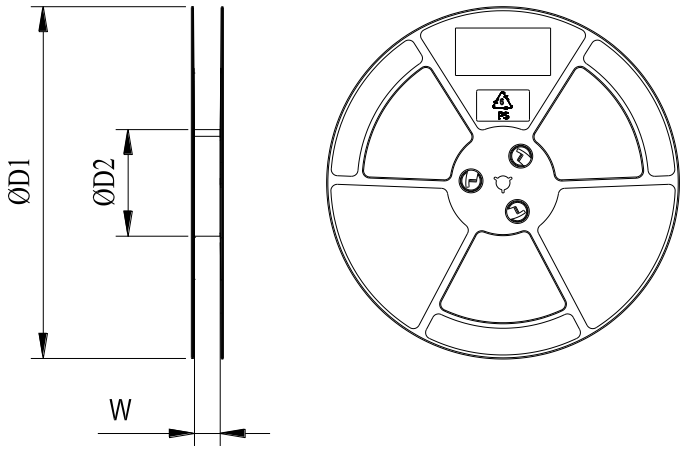
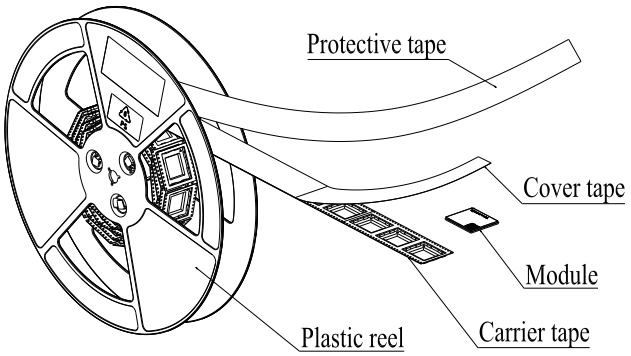


Figure 48: Plastic Reel Dimension Drawing

Table 41: Plastic Reel Dimension Table (Unit: mm)

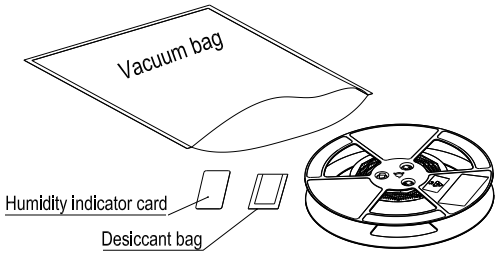
øD1	øD2	W
330	100	32.5

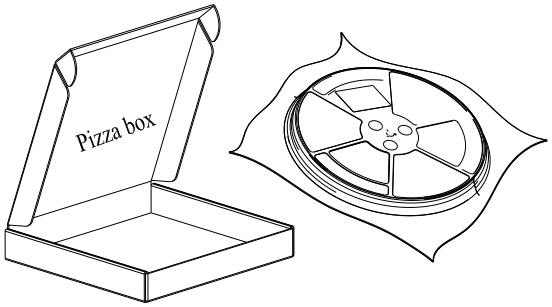
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 1000 modules.

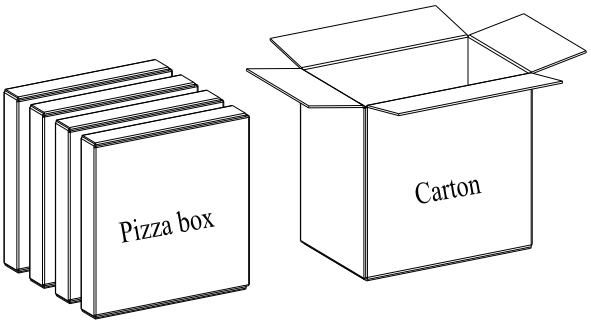


Figure 49: Packaging Process

9 Appendix References

Table 42: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_LTE_Standard(A)_Series_AT_Commands_Manual
[3] Quectel_LTE_Standard(A)_Series_Audio_Application_Note
[4] Quectel_EC800M-CN_Reference_Design
[5] Quectel_EC200N-CN&EC800M-CN&EG915N_Series_GNSS_Application_Note
[6] Quectel_RF_Layout_Application_Note
[7] Quectel_Module_Secondary_SMT_Application_Note

Table 43: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
AMR	Adaptive Multi-Rate
ASM	Antenna Switch Modules
BDS	BeiDou Navigation Satellite System
bps	Bits per second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection MUX
CPE	Customer-Premise Equipment
CTS	Clear To Send

DCS	Data Coding Scheme
DFOTA	Delta Firmware Upgrade Over-The-Air
DTE	Data Terminal Equipment
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplexing
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP over SSL
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russia)
GND	Ground
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IMS	IP Multimedia Subsystem
IMU	Inertial Measurement Unit
LCC	Leadless Chip Carrier (package)
LDO	Low-dropout Regulator

LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MCU	Microcontroller Unit
ME	Mobile Equipment
MLCC	Multi-layer Ceramic Capacitor
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
NITZ	Network Identity and Time Zone
NMEA	National Marine Electronics Association
NTP	Network Time Protocol
OTT	Over The Top
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper
PMU	Power Management Unit
POS	Point of Sale
PPP	Point-to-Point Protocol
RAM	Random Access Memory
RF	Radio Frequency

RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SAW	Surface Acoustic Wave
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDD	Time Division Duplexing
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
USIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}	High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}	Low-level Input Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio