

EG91xQ Series Reference Design

LTE Standard Module Series

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Quectel Wireless Solutions Co., Ltd.

Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China

Tel: +86 21 5108 6236 Email: <u>info@quectel.com</u>

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About the Document

Revision History

Version	Date	Author	Description
-	2023-02-10	Lex LI	Creation of the document
1.0	2023-03-14	Lex LI	First official release
1.1	2023-09-22	Lex LI	 Added the applicable module EG916Q-GL. Updated the following pins: pin 25: from SPI_CS to RESERVED; pin 26: from SPI_CLK to RESERVED; pin 27: from SPI_MOSI to GNSS_TXD; pin 28: from SPI_MISO to GNSS_RXD; pin 49: from RESERVED to ANT_GNSS; pin 51: from RESERVED to GNSS_PPS; pin 84: from RESERVED to USIM2_CLK; pin 85: from RESERVED to USIM2_RST; pin 86: from RESERVED to USIM2_DATA; pin 87: from RESERVED to USIM2_VDD; pin 109: from RESERVED to GNSS_DBG_TXD; pin 110: from RESERVED to GNSS_DBG_RXD; pin 117: from RESERVED to GNSS_PWR_EN; pin 118: from RESERVED to GNSS_VBCKP. Added GNSS related reference design. Added the reference design of USIM2 interface (Sheet 7).
1.2	2024-08-07	Fanny CHEN/ Lem JIN	 Added the applicable modules EG915Q-AF and EG915Q-JP. Updated the current that is provided to the module from 2.0 A to 1.5 A (Sheets 1 & 5). Added Wi-Fi Scan function (Sheets 1 and 8).



- 4. Updated test points (Sheets 1 & 9).
- Added two notes about GNSS design guidelines;
 Added the reference design of ADC interfaces (Sheet 3).
- 6. Updated the reference design of antenna interfaces (Sheet 8).



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1 Reference Design

1.1. Introduction

This document provides the reference design for Quectel EG91xQ series. The reference design mainly includes the block diagram, power system block diagram, module interfaces, MCU interfaces, power supply design, UARTs and USIM interface design, antenna interface design and other designs.

This document is applicable to the following modules:

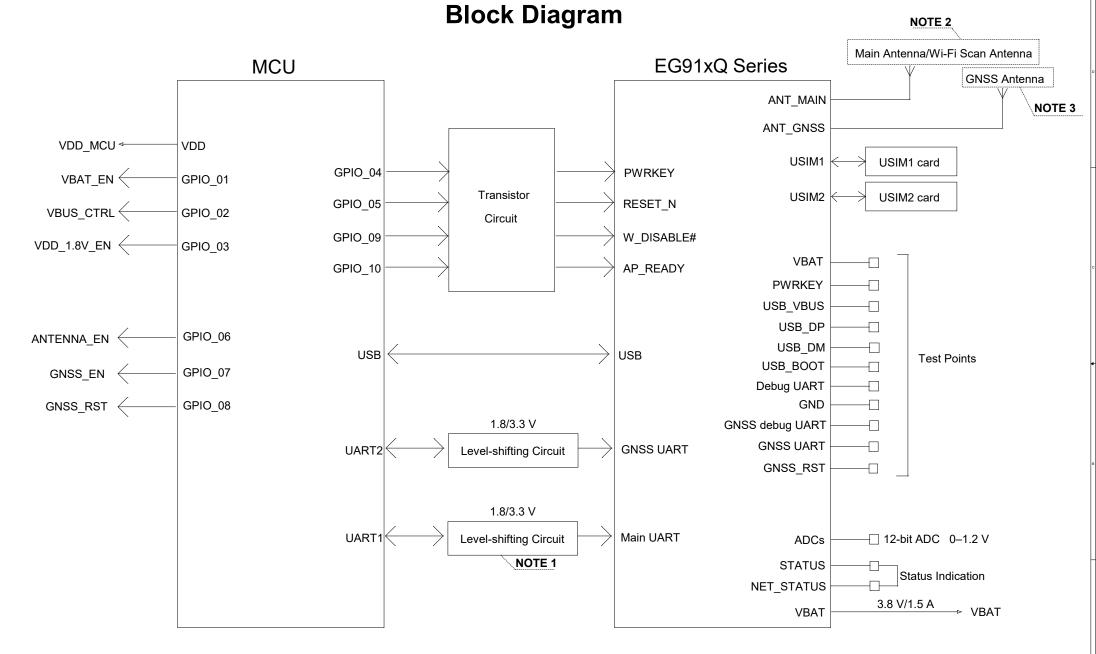
- EG915Q Series (EG915Q-NA, EG915Q-AF and EG915Q-JP)
- EG916Q-GL

1.2. Schematics

The schematics illustrated in the following pages are provided for reference only.

NOTE

It is required to confirm the applicability and price from the supplier about the IC involved in the reference design.

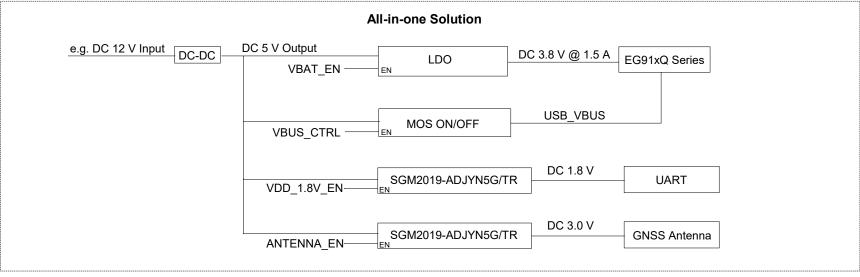


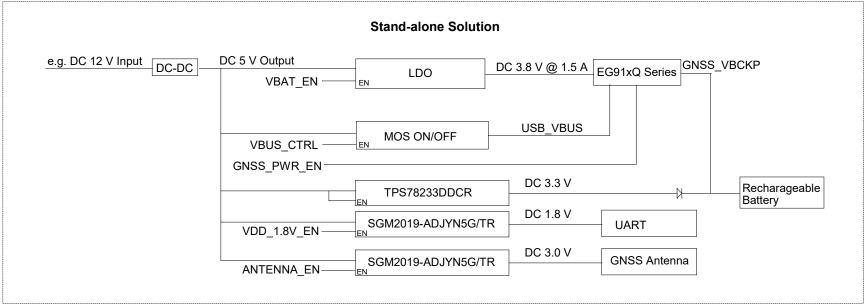
NOTE:

- $1.\ A\ transistor\ solution\ or\ an\ IC\ solution\ TXS0108 EPWR\ provided\ by\ Texas\ Instruments\ is\ recommended.$
- 2. Wi-Fi scan function is optional. This function and LTE network cannot be used simultaneously since they share the same antenna interface.
- 3. GNSS interface is optional. If you need this function, please contact Quectel Technical Support.

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Power System Block Diagram



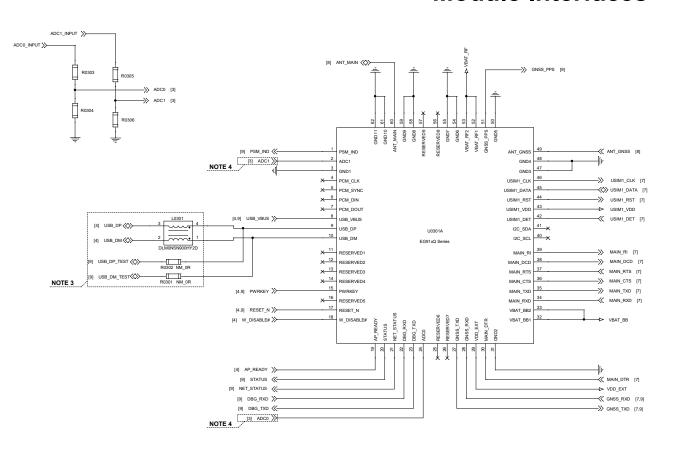


NOTE:

EG91xQ series integrates both LTE and GNSS engines which can work as a whole (All-in-one solution) unit or work independently (Stand-alone solution) according to your demands.

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Module Interfaces



// GNSS RST M 01 × 104 RESERVED11 RESERVED20 X 63 RESERVED12 CAM_SPI_CLK X 64 RESERVED13 GRFC2 X 65 NOTE 13 RESERVED14 GRFC1 ₩ usb_boot [9] FG91xO Series GND19 X 105 RESERVED16 GNSS_DBG_RXD -≪ GNSS_DBG_RXD [9] X 106 RESERVED17 ->> GNSS DBG TXD 191 GNSS DBG TXD SNSS VBCKP CAM PWDN GNSS VBCKE X 83 CAM_SPI_DATA1 98_X RESERVED23 NOTE 10 & 12 CAM_SPI_DATA0 97 X USIM2_CLK I71 USIM2 RST <<-USIM2 RST PSM INT ✓ PSM INT 191 CAM_MCLK 95 × [7] USIM2_DATA (>> USIM2 DATA CAM_VDD 94 X LISIM2 VDD <-USIM2 VDD CAM_VDDIO 93 X X 88 RESERVED24 X 116 RESERVED25 - GNSS_PWR_EN [4]

× 120

x 121

RESERVED29 RESERVED34

RESERVED30 RESERVED33
RESERVED31 RESERVED32

EG91xQ Series

NOTE:

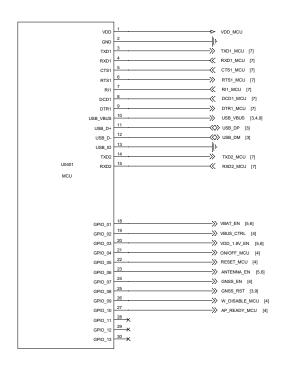
- 1. All GND pins should be connected to ground, and keep unused and RESERVED pins unconnected.
- 2. If the module does not need to enter forced download mode, USB_BOOT (pin 75) should not be pulled up to VDD_EXT before the module successfully starts up.
- 3. A common mode choke L0301 is recommended to be added in series between the module and your MCU to suppress EMI, and it should be placed close to the module.
 Meanwhile, test points of USB interface must be reserved, which can be used for firmware upgrading and debugging. Keep extra stubs of the trace as short as possible.
 R0301 and R0302 should be placed close to the module to ensure the integrity of USB signals.
- 4. The input voltage range of the ADC interfaces is 0–1.2 V. When the collected voltage is higher than 1.2 V, it is recommended to use the resistor divider circuit for ADC application.

The divider resistor accuracy should not exceed 1 %, and the resistance should not exceed 100 kΩ. It is recommended to reserve a 100 nF capacitor for the design.

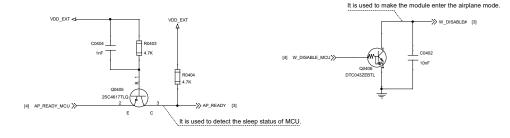
- 5. In sleep mode, pins 34–37 of the main UART interface, pins 22 and 23 of debug UART interface, USB_BOOT (pin 75), pins 4–7 of PCM interface, pins 40 and 41 of I2C interface, pins 22 and 23 of debug UART interface, USB_BOOT (pin 75), pins 4–7 of PCM interface, pins 40 and 41 of I2C interface, pi
- 6. When USIM1 and USIM2 are used at the same time, the power domain of USIM interfaces should be 1.8 V. Otherwise, USIM2 interface will be damaged.
- 7. The module supports SPI interface. If you need this function, please contact Quectel Technical Support.
- 8. GNSS interface (pins 27, 28, 49, 51, 109, 110, 112, 117, 118) is optional. If you need this function, please contact Quectel Technical Support.
- 9. USIM2 and Camera SPI interfaces cannot be used at the same time.
- 10. In All-in-one solution, GNSS PWR EN, GNSS VBCKP can be unconnected.
- 11. Whether in Stand-alone or All-in-one solution, to facilitate updating GNSS firmware, it is highly recommended to reserve test points for GNSS UART (pins 27 and 28) and GNSS_RST (pin 112).
- 12. In the Stand-alone or All-in-one solution, if the GNSS chip is powered externally, the GNSS firmware cannot be upgraded through the LTE network because LTE cannot reset the GNSS chip. If you want to upgrade the GNSS firmware through the LTE network, you need to disconnect GNSS_PWR_EN (pin 117) and GNSS_VBCKP (pin 118) from the outside or set both pins to low.
- 13. If you need GRFC function, please contact Quectel Technical Support for the related reference design.

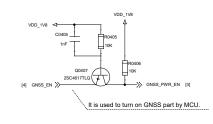


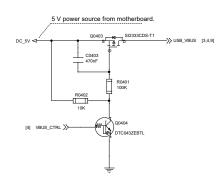
MCU Interface Design











NOTE

1. U0401 represents your MCU. The power domain of GPIO interfaces of the module is 1.8 V.

If the power domain of GPIO interfaces of U0401 is also 1.8 V, then the related level-shifting circuit is not needed.

2. The USB interface of the module only serves as a slave device and supports high-speed and full-speed modes of USB 2.0.

To communicate with the USB interface, MCU needs to support USB host mode or OTG function.

The USB_VBUS pin of the module should be powered by an external power system for USB detection, and VBUS_CTRL is used to turn on/off the USB_VBUS power supply.

3. It is recommended to select the GPIO pins of MCU, which are at low level by default, as the control pins for PWRKEY and RESET_N of the module.

Ensure that the load capacitance does not exceed 10 nF on PWRKEY and RESET_N pins.

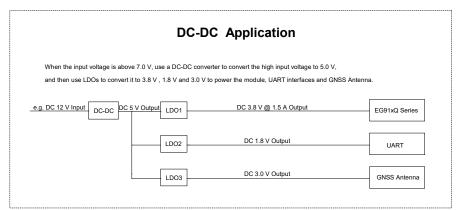
4. When the sleep function of the module is enabled, pulling down MAIN_DTR can wake up the module from the sleep mode.

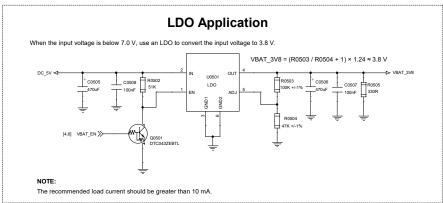
For details of the AT commands for configuration, see the hardware design document of the module.

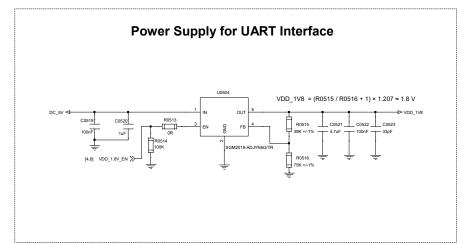
You can choose the level-shifting circuit on Sheet "UARTs and USIM Interface Design".

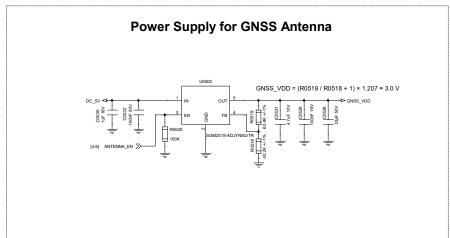
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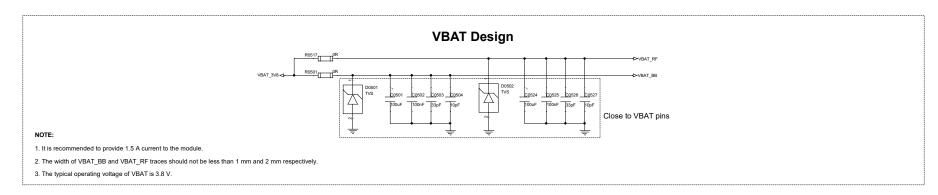
Power Supply Design (All-in-one Solution)





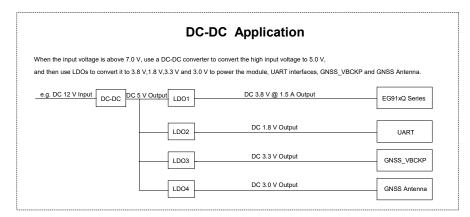


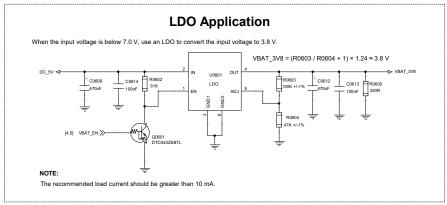


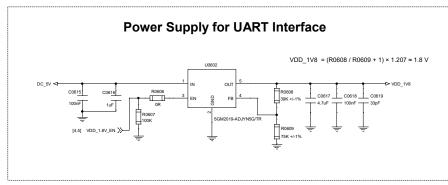


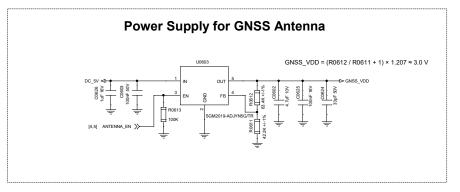


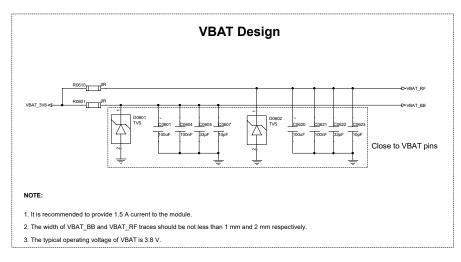
Power Supply Design (Stand-alone Solution)

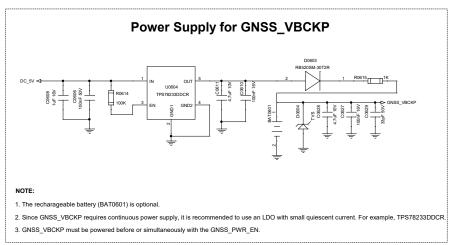






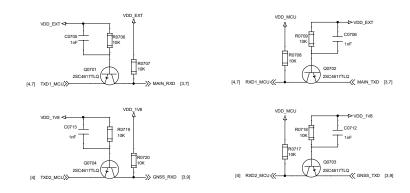




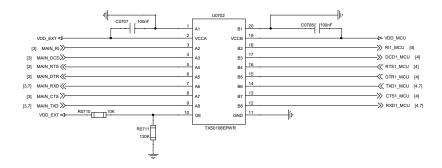


UARTs and USIM Interface Design

UART Level-shifting Circuit - Transistor Solution



UART Level-shifting Circuit - IC Solution



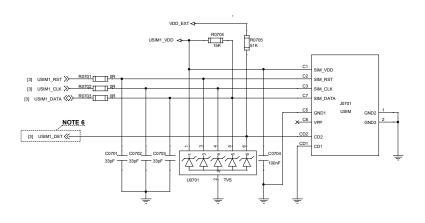
NOT

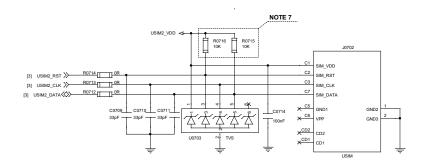
- 1. There are two level-shifting solutions: transistor solution and IC solution, and it is recommended to select the latter one
- 2. The power supply of TXS0108EPWR's VCCA should not exceed that of VCCB. For more information, see the datasheet of TXS0108EPWR.
- 3. The transistor solution is not suitable for applications with baud rates exceeding 460 kbps.

The 1 nF capacitors can improve the signal quality.

- 4. The level-shifting circuit of MAIN RTS is similar to that of MAIN RXD.
- The level-shifting circuits of MAIN_CTS, MAIN_RI and MAIN_DCD are similar to that of MAIN_TXD.
- 5. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

USIM Interface Design





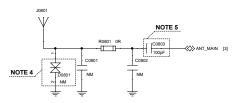
NOTE

- 1. When USIM1 and USIM2 are used at the same time, the power domain of USIM interfaces should be 1.8 V. Otherwise, USIM2 interface will be damaged.
- 2. U0701 and U0703 is recommended to be used to offer good ESD protection, and the parasitic capacitance should be less than 15 pF.
- 3. The pull-up resistor R0704, R0715 and R0716 can improve anti-jamming capability, and should be placed close to the USIM card connector.
- 4. The capacitance of C0704 and C0714 should be less than 1 μF and it should be placed close to the USIM card connector.
- 5. R0701-R0703, R0712-R0714 are used for debugging, and C0701-C0703, C0709-C0711 are used for filtering out RF interference.
- 6. Only USIM1 supports hot-plug detection.
- 7. When only USIM1 interface is used, please make sure that these two 10K resistors are not mounted. Otherwise, USIM2 interface may be damaged.
- 8. USIM2 and Camera SPI interfaces cannot be used at the same time

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Antenna Interface Design

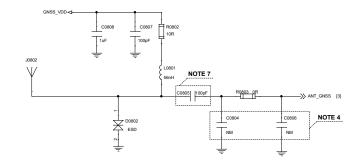
LTE/Wi-Fi Scan Antenna Interface



NOTE:

- 1. The single-ended impedance of the RF antenna is 50 Ω .
- 2. It is highly recommended to reserve a dual L-type matching circuit for main antenna for future debugging.
- 3. The impedance of RF signal traces must be controlled as 50 Ω when routing.
- 4. It is recommended to reserve an ESD protection component for the cellular antenna interface and the junction capacitance should not exceed 0.05 pF.
- 5. If there is DC power at the antenna ports, C0803 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C0803 should not be reserved.

GNSS Antenna Interface



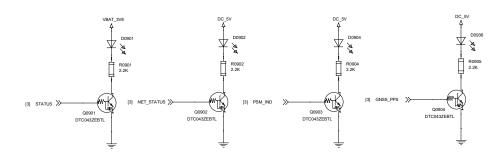
NOTE:

- 1. An external LDO can be selected according to the active antenna requirement.
- 2. If passive antenna is used, then C0808, C0807,R0802 and L0801 are not mounted.
- 3. The impedance of RF signal traces must be controlled as 50 Ω when routing.
- 4. C0804 and C0806 are reserved for impedance matching and attenuation circuits.
- 5. The module's GNSS function is optional
- 6. It is recommended to reserve an ESD protection component for the antenna interface and the junction capacitance should not exceed 0.05 pF.
- 7. For passive antenna, if there is DC power at the antenna ports, C0805 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C0805 should not be reserved.

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Other Designs

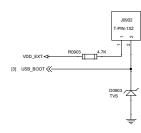
Indicators



NOTE

If your device has low power consumption requirements in sleep mode, replace the power supplies (VBAT_3V8 and DC_5V) of STATUS, NET_STATUS, PSM_IND and GNSS_PPS with external controllable ones. Turn off the power when the module is in sleep mode to reduce the power consumption.

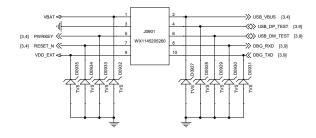
Download Interface



NOTE:

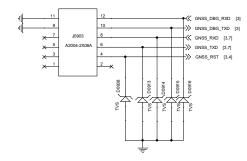
- 1. A test point for USB_BOOT must be reserved.
- Pulling up USB_BOOT to VDD_EXT before turning on the module, and then the module will enter forced download mode, in which the module supports firmware upgrade over USB 2.0 interface.

Reserved Test Points



NOTE

- Test points of USB_VBUS, USB_DP/DM, debug UART, GNSS debug UART and USB_BOOT must be reserved.
 Test points of VBAT_BB, VBAT_RF, VDD_EXT, PWRKEY, GNSS UART and GNSS_RST are recommended to be reserved.
 A test point of RESET_N is recommended to be reserved if unused.
- 2. Test points of debug UART interfaces are reserved for the output of partial logs.
- 3. Test points of USB interface are used for firmware upgrading, debugging and output of partial logs.
- 4. The stray capacitance of the ESD protection components on USB data traces should be less than 2 pF for USB 2.0.
- 5. The debug UART interface supports 1.8 V power domain, and a level-shifting circuit should be used if the power domain of your application is 3.3 V.
- 6. Whether in Stand-alone or All-in-one solution, to facilitate GNSS firmware upgrade, it is recommended to reserve test points for GNSS UART (pins 27 and 28) and GNSS_RST (pin 112).



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