EG91xQ&BG9x&EG9x Series

Compatible Design

LTE Standard & LPWA Module Series

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About the Document

Revision History

Version	Date	Author	Description
-	2023-03-03	Lex LI/Joe MA	Creation of the document
1.0	2023-05-12	Lex LI/Olina CAO/ Barry DENG/ Pearl GUO	First official release
1.1	2023-12-12	Lex LI/ Soley ZHANG/ Barry DENG/ Daisy ZHU/ Lonely WANG/ Sean FANG	1. Added an applicable module EG916Q-GL. 2. Updated the following pins of EG91xQ family module: pin 25: from SPI_CS to RESERVED. pin 26: from SPI_CLK to RESERVED. pin 27: from SPI_MOSI to GNSS_TXD. pin 28: from SPI_MISO to GNSS_RXD. pin 49: from RESERVED to ANT_GNSS. pin 51: from RESERVED to GNSS_PPS. pin 84: from RESERVED to USIM2_CLK. pin 85: from RESERVED to USIM2_RST. pin 86: from RESERVED to USIM2_DATA. pin 87: from RESERVED to USIM2_VDD. pin 109: from RESERVED to GNSS_ DBG_TXD. pin 110: from RESERVED to GNSS_ DBG_RXD. pin 112: from RESERVED to GNSS_RST. pin 117: from RESERVED to GNSS_PWR_EN. pin 118: from RESERVED to GNSS_VBCKP. 3. Updated the VBAT_RF's peak current of BG96 (Tables 6 & 9).

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1 Introduction

Quectel LTE Standard EG9x family (EG91 series and EG95 series), EG915Q-NA and EG916Q-GL are compatible with LPWA BG9x family (BG95 series and BG96). This document outlines the compatible design among these modules.

NOTE

Blue text indicates the differences among BG9x family, EG9x family, EG915Q-NA and EG916Q-GL, unless otherwise specified.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument, and so on, it indicates that the function, feature, interface, pin, AT command, argument, and so on, is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

1.2. Applicable Modules

Table 2: Applicable Modules

Product Line	Module Family	Module Series	Model
LTE Standard	EG91xQ	-	EG915Q-NA
		-	EG916Q-GL
	EG9x	EG91	EG91-AUX/-E/-EX/-JP/-NA/-NAX/-NAXD/-VX
		EG95	EG95-AUX/-E/-EX/-JP/-NA/-NAX/-NAXD
LPWA	BG9x	BG95	BG95-M1/-M2/-M3/-M4/-M5/-M6/-MF/-M8/-M9
		-	BG96

2 General Description

2.1. Product Description

BG95 is a series of embedded IoT (LTE Cat M1/Cat NB2 [1]/EGPRS) wireless communication modules. It supports data connectivity on LTE HD-FDD and GPRS/EGPRS networks. It also provides GNSS and voice functionalities to meet your specific application demands.

BG96 is an embedded IoT (LTE Cat M1/Cat NB1/EGPRS) wireless communication module. It supports data connectivity on LTE HD-FDD and GPRS/EGPRS networks, and half-duplex operation in LTE networks. It also features GNSS and voice functionalities to meet your specific application demands.

EG91 series and EG95 series modules are embedded 4G wireless communication modules with Rx-diversity, supporting LTE, WCDMA, GSM wireless communication, and providing data connectivity on LTE-FDD, LTE-TDD [2], DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, EDGE and GPRS networks. They can also provide GNSS and voice [3] functionalities.

EG915Q-NA and EG916Q-GL are LTE Standard wireless communication modules. They support data connectivity on LTE network, Wi-Fi scan and GNSS to meet your specific application demands.

NOTE

For detailed information on the supported networks of the applicable modules, see ***Table 3***.

Table 3: Supported Networks of the Modules

Module	LTE-FDD	LTE-TDD	WCDMA	GPRS/EGPRS
BG95 series	LTE-HD-FDD	-	-	Supported on BG95-M3/-M5/-M8
BG96	LTE-HD-FDD	-	-	√

[1] LTE Cat NB2 is backward compatible with LTE Cat NB1.
[2] LTE-TDD does not supported on EG91 series.
[3] EG9x family modules contain the **Data + Voice** version and the **Data-only** version.

EG91 series	√	-	Supported on EG9x-AUX/-E/ -EX/-NA/-NAX/ -NAXD	Supported on EG9x-AUX/-E/-EX
EG95 series	√	Supported on EG95-JP		
EG915Q-NA	√	-	-	-
EG916Q-GL	√	√	-	-

Table 4: Supported Module Functions

Module	Voice Functionality	Wi-Fi Scan	GNSS
BG95 series	√	Supported on BG95-MF	√
BG96	√	-	○
EG9x family	○	-	○
EG91xQ family	-	√	○

NOTE

1. "√" means supported.
2. "-" means not supported.
3. "○" means optional.
4. BG95 series module supports VoLTE* (Voice over LTE) under LTE Cat M1, but this function in BG95-MF and BG95-M9 is under development. Additionally, BG95-M3 and BG95-M5 also support CS voice under GSM.
5. BG96 supports VoLTE (Voice over LTE) under LTE Cat M1 network.
6. For EG91xQ family, Wi-Fi scan function and LTE network cannot be use simultaneously since they share the same antenna interface.

2.1.1. General Information

Table 5: General Information

Module	Appearance	Packaging	Dimensions (mm)	Description
BG95 series		102 LGA pins	23.6 × 19.9 × 2.2	LPWA module
BG96		102 LGA pins	26.5 × 22.5 × 2.3	LPWA module
EG91 series		106 LGA pins	**EG91-E:** 29.0 × 25.0 × 2.3 **EG91-AUX/-EX/ -JP/-NA/-NAX/ -NAXD/-VX:** 29.0 × 25.0 × 2.45	LTE Standard module
EG95 series		106 LGA pins	**EG95-E:** 29.0 × 25.0 × 2.3 **EG95-AUX/-EX/ -JP/-NA/-NAX/ -NAXD:** 29.0 × 25.0 × 2.45	LTE Standard module
EG915Q-NA		126 LGA pins	23.6 × 19.9 × 2.4	LTE Standard module

EG916Q-GL		126 LGA pins	26.5 × 22.5 × 2.4	LTE Standard module

2.2. Feature Overview

The key features are compared in the table below.

Table 6: Feature Overview

Feature	BG95 Series	BG96	EG9x Family	EG91xQ Family
Power Supply	**BG95-M1/-M2:** ● Supply voltage [4]: 2.6–4.8 V ● Typical supply voltage: 3.3 V **BG95-M3/-M5/-M6/-MF/-M8:** ● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V **BG95-M4/-M9:** ● Supply voltage: 3.2–4.2 V ● Typical supply voltage: 3.8 V	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Peak Current	**VBAT_BB:** Max. 0.6 A **VBAT_RF:** Max. 2.7 A	**VBAT_BB:** Max. 0.5 A **VBAT_RF:** Max. 2.7 A	**VBAT_BB:** Max. 0.8 A **VBAT_RF:** Max. 1.8 A	**VBAT_BB:** 0.5 A **VBAT_RF:** 1.5 A
Sleep Current	**LTE Cat M1 @ DRX = 1.28 s:** 1.7 mA @ BG95-M1 1.68 mA @ BG95-M2 1.89 mA @ BG95-M3 1.53 mA @ BG95-M4 1.56 mA @ BG95-M5 1.42 mA @ BG95-M6 1.59 mA @ BG95-MF 1.56 mA @ BG95-M8 1.37 mA @ BG95-M9 **LTE Cat NB1 @ DRX = 1.28 s:** 1.55 mA @ BG95-M2 1.49 mA @ BG95-M3 1.39 mA @ BG95-M4 1.43 mA @ BG95-M5 1.31 mA @ BG95-M6 1.43 mA @ BG95-MF 1.51 mA @ BG95-M8	**LTE Cat M1 @ DRX = 1.28 s:** 1.54 mA **LTE Cat NB1 @ DRX = 1.28 s:** 2.03 mA	**WCDMA PF = 64 (USB disconnected):** 1.8 mA @ EG91-AUX/-EX, EG95-E/-EX 1.7 mA @ EG91-E, EG95-AUX 2.2 mA @ EG91-NA, EG95-NA 2.1 mA @ EG91-NAX/-NAXD 2.0 mA @ EG95-NAX/-NAXD **LTE PF = 64 (USB disconnected):** 2.2 mA @ EG95-AUX 2.3 mA @ EG91-AUX/-EX, EG95-E/-EX 2.1 mA @ EG91-E 1.9 mA @ EG91-JP 2.6 mA @ EG9x-NA/-NAX/-NAXD 2.4 mA @ EG91-VX 2.0 mA @ EG95-JP	**LTE PF = 64 (USB disconnected):** 0.68 mA @ EG915Q-NA 0.68 mA @ EG916Q-GL

[4] For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full functionality mode, the minimum power supply voltage should be higher than 2.8 V.

	1.36 mA @ BG95-M9			
Temperature Range	● Operating temperature range [5]: -35 to +75 °C ● Extended temperature range [6]: -40 to +85 °C ● Storage temperature range: -40 to +90 °C			
UART Interfaces	**Main UART:** ● Used for data transmission and AT command communication. ● Baud rate: 115200 bps by default. ● Default frame format: 8N1 (8 data bits, no parity, 1 stop bit). ● RTS and CTS hardware flow control. **Debug UART:** ● Used for software debugging and log output. ● Baud rate: fixed at 115200 bps. **GNSS UART:** ● Used for GNSS data and GNSS NMEA sentence output. ● Baud rate: 115200 bps by default.	**UART1:** ● Used for data transmission and AT command communication. ● Baud rate: 115200 bps by default. ● Default frame format: 8N1 (8 data bits, no parity, 1 stop bit). ● RTS and CTS hardware flow control. **UART2:** ● Used for software debugging and log output. ● Baud rate: 115200 bps. **UART3:** ● Used for GNSS data or GNSS NMEA sentence output. ● Baud rate: 115200 bps.	**Main UART:** ● Used for data transmission and AT command communication. ● Baud rate: up to 921600 bps, 115200 bps by default. ● RTS and CTS hardware flow control. **Debug UART:** ● Used for Linux console and log output. ● Baud rate: 115200 bps.	**Main UART:** ● Used for data transmission and AT command communication. ● Baud rate: 115200 bps by default. ● RTS and CTS hardware flow control. **Debug UART:** ● Used for partial log output. ● Baud rate: up to 3 Mbps, 115200 bps by default. **GNSS UART:** ● Used for GNSS data and GNSS NMEA sentence output. ● Baud rate: 921600 bps by default. **GNSS debug UART:** ● Used for GNSS system log output ● Baud rate: 3 Mbps
USB Interface	● Compliant with USB 2.0 specification (slave only). ● Data transfer rate: up to 480 Mbps. ● Supports high-speed, low-speed and full-speed modes. ● Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging and firmware upgrade. ● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–6.5, Android 4.x–13.x.	● Compliant with USB 2.0 specification (slave only). ● Data transfer rate: up to 480 Mbps. ● Supports high-speed and full-speed modes. ● Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging and firmware upgrade. ● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–6.5, Android 4.x–13.x.	● Compliant with USB 2.0 specification (slave only). ● Data transfer rate: up to 480 Mbps. ● Supports high-speed and full-speed modes. ● Used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB. ● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–6.5, Android 4.x–13.x.	● Compliant with USB 2.0 specification (slave only). ● Data transfer rate: up to 480 Mbps. ● Supports high-speed and full-speed modes. ● Used for AT command communication, data transmission, GNSS NMEA sentence output (**All-in-one** mode only), software debugging, firmware upgrade and the output of partial logs. ● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–6.5, Android 4.x–13.x.
Digital Audio Interface	PCM interface [7] for VoLTE* or GSM CS voice	PCM interface for VoLTE only	PCM interface	PCM interface*
I2C Interface	I2C interface [7] for VoLTE* or GSM CS voice	I2C interface for VoLTE only	I2C interface	I2C interface*
(U)SIM Interface	1.8 V (U)SIM	1.8/3.0 V (U)SIM	1.8/3.0 V (U)SIM	● USIM1: 1.8/3.0 V ● USIM2: 1.8 V

[5] Within the operating temperature range, the module meets 3GPP specifications.
[6] Within the extended temperature range, the module retains the ability to establish and maintain functions such as voice (The voice function is only supported for BG95 series, BG96 and EG9x family, and is under development for BG95-MF/-M8/-M9), SMS, data transmission, emergency call (only for BG96), etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[7] The VoLTE function* of the PCM and I2C interfaces is under development for BG95-MF/-M9.

Wi-Fi Scan	2.4 GHz (BG95-MF only)	-	-	2.4 GHz
Firmware Upgrade	● USB interface ● DFOTA			

3 Pin Definition

3.1. Pin Assignment

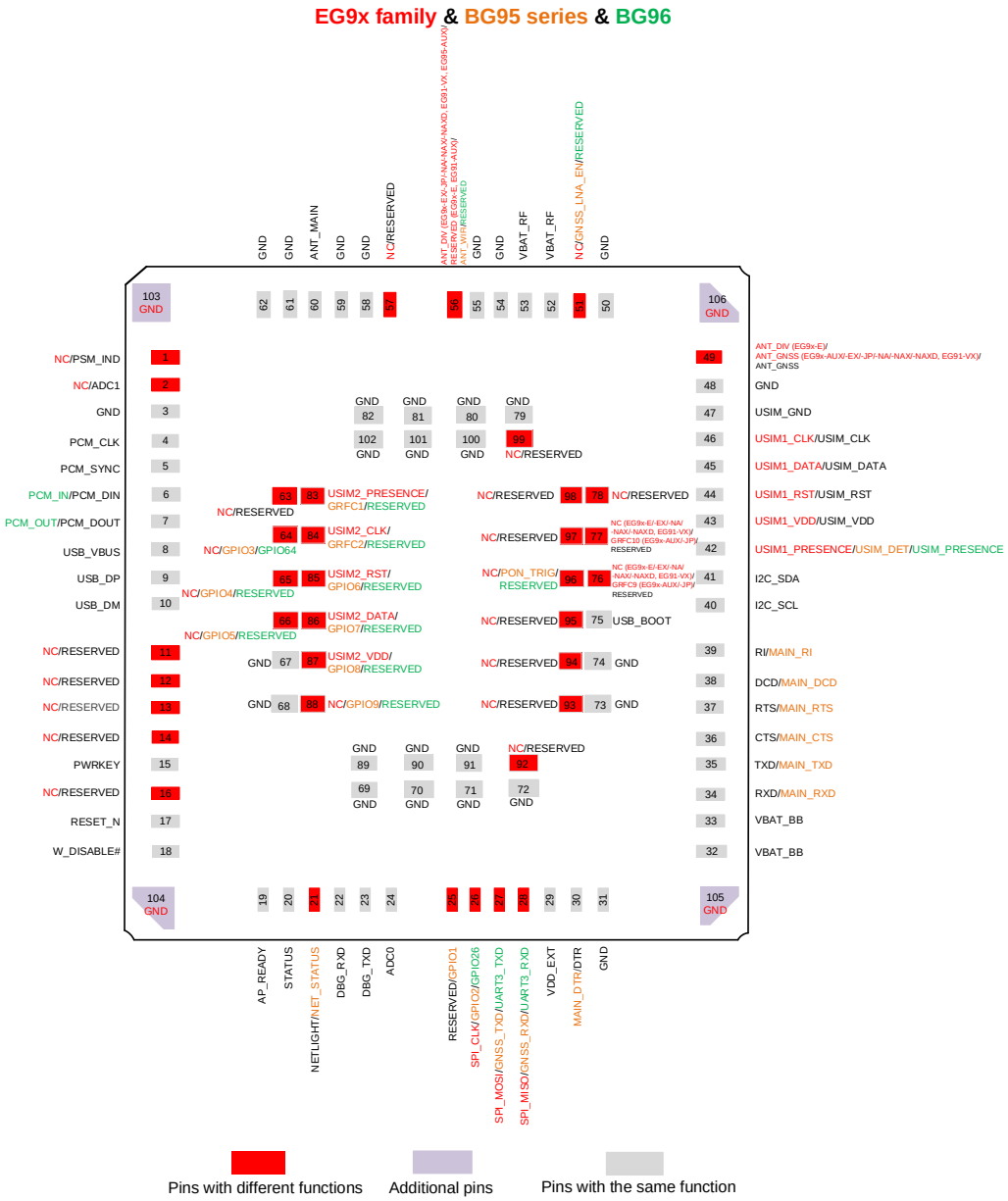


Figure 1: Pin Assignment of BG9x & EG9x Family (Top View)

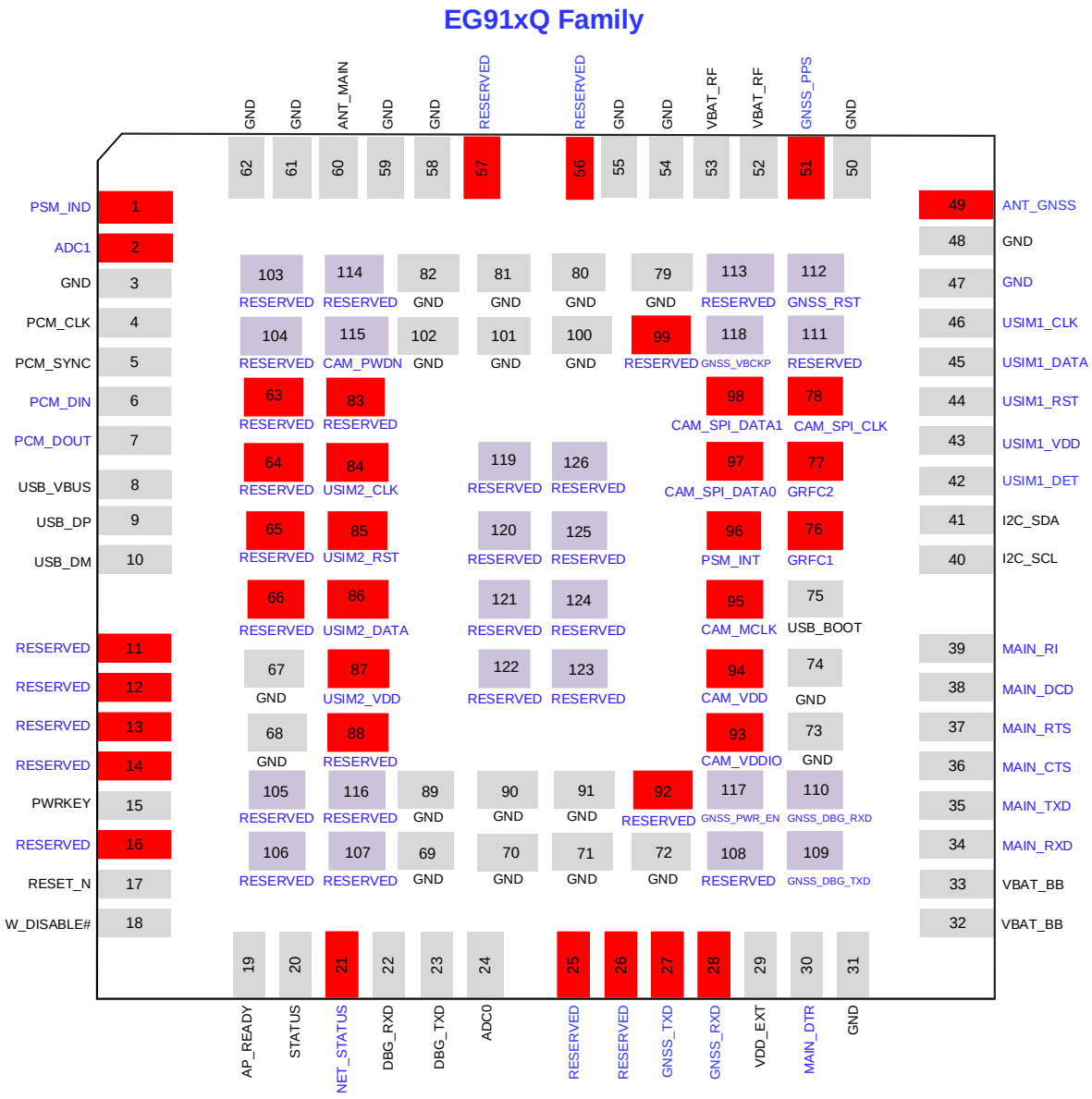


Figure 2: Pin Assignment of EG91xQ Family (Top View)

NOTE

1. Keep all RESERVED, NC and unused pins unconnected.
2. Connect GND pins to the ground in the design.
3. For BG96 and EG9x family, PWRKEY output voltage is 0.8 V because of the diode voltage drop inside the chipset.
4. **BG95 series:**
   - PWRKEY output voltage is 1.5 V because of the voltage drop inside the chipset. Due to platform-related reasons, the reset function is integrated into PWRKEY on the chipset. Therefore, never pull down PWRKEY to GND permanently.

- Supports ADC0 and ADC1. Do not use ADC0 and ADC1 simultaneously, as ADC1 is directly connected to ADC0 inside the module. If you need to use the two ADC interfaces at the same time, add an external analog switch.
- **BG95-MF:**
  - Only BG95-MF supports ANT_WIFI (pin 56).
  - Does not support GPIO3 and GPIO4 interfaces (pins 64 and 65).
- Only **BG95-M4/-MF** support GNSS_LNA_EN (pin 51).
- **BG95-M4/-M8/-M9** do not support GRFC interfaces (pins 83 and 84).
- GNSS_TXD (pin 27) and GRFC2 (pin 84) and GNSS_LNA_EN (pin 51) are BOOT_CONFIG pins. Never pull them up before startup, otherwise the module cannot power on normally.
- GPIO1 (pin 25) supports fast shutdown function, which is disabled by default.
- PCM and I2C interfaces are used for VoLTE or GSM CS voice.

5. **EG9x family:**
   - Supports Dual SIM Single Standby function.
   - BOOT_CONFIG pins (SPI_CLK, USB_BOOT, PCM_CLK, PCM_SYNC) cannot be pulled up before startup.
   - **EG91 series:**
     - Pin 49 is defined as ANT_GNSS on EG91-AUX/-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as ANT_DIV on EG91-E.
     - Pin 56 is defined as ANT_DIV on EG91-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as RESERVED on EG91-AUX/-E. Rx-diversity antenna is not supported on EG91-AUX.
     - Pins 76 and 77 are respectively defined as GRFC9 and GRFC10 on EG91-AUX/-JP, while they are defined as NC on EG91-E/-EX/-NA/-NAX/-NAXD/-VX.
   - **EG95 series:**
     - Pin 49 is defined as ANT_GNSS on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as ANT_DIV on EG95-E.
     - Pin 56 is defined as ANT_DIV on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as RESERVED on EG95-E.
     - Pins 76 and 77 are respectively defined as GRFC9 and GRFC10 on EG95-AUX/-JP, while they are defined as NC on EG95-E/-EX/-NA/-NAX/-NAXD.
6. **EG91xQ family:**
   - If the module does not need to enter download mode, USB_BOOT (pin 75) should not be pulled up to VDD_EXT before the module successfully starts up.
   - In sleep mode, pins 34–37 of the main UART interface, pins 22 and 23 of debug UART interface, USB_BOOT (pin 75), pins 4–7 of PCM interface*, pins 40 and 41 of I2C interface*, and pins 78, 93, 95, 97, 98 and 115 of Camera SPI* are powered down. The driving capacity will be lost and the status indication and data transmission functions are disabled. Pay attention to it when designing circuits.
   - When USIM1 and USIM2 are used at the same time, the power domain of USIM interfaces should be 1.8 V. Otherwise, USIM2 interface will be damaged.
   - The module supports SPI. If you need this function, please contact Quectel Technical Support.
   - GNSS interface (Pins 27, 28, 49, 51, 109, 110, 112, 117, 118) is optional. If you need this function, please contact Quectel Technical Support.
   - USIM2 and Camera SPI* cannot be used at the same time.

Table 7: I/O Parameter Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

3.2. Pin Comparison

The following table describes the pin functions, I/O and DC characteristics of BG9x family, EG9x family, and EG91xQ family.

Table 8: Pin Comparison

Pin No.	BG95 Series			BG96			EG9x Family			EG91xQ Family			Description
	Pin Name	I/O	Power Domain	Pin Name	I/O	Power Domain	Pin Name	I/O	Power Domain	Pin Name	I/O	Power Domain	
1	PSM_IND [8]	DO	1.8 V	PSM_IND [8]	DO	1.8 V	NC	-	-	PSM_IND*	DO	1.8 V	1. Indicate the module's power saving mode. 2. Not connected.
2	ADC1	AI	0.1–1.8 V	ADC1	AI	0.3–1.8 V	NC	-	-	ADC1	AI	0–1.2 V	1. General-purpose ADC interface. 2. Not connected.
3	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
4	PCM_CLK	DO	1.8 V	PCM_CLK	DO	1.8 V	PCM_CLK	DIO	1.8 V	PCM_CLK*	DO	1.8 V	PCM clock.
5	PCM_SYNC	DO	1.8 V	PCM_SYNC	DO	1.8 V	PCM_SYNC	DIO	1.8 V	PCM_SYNC*	DO	1.8 V	PCM data frame sync.
6	PCM_DIN	DI	1.8 V	PCM_IN	DI	1.8 V	PCM_DIN	DI	1.8 V	PCM_DIN*	DI	1.8 V	PCM data input.
7	PCM_DOUT	DO	1.8 V	PCM_OUT	DO	1.8 V	PCM_DOUT	DO	1.8 V	PCM_DOUT*	DO	1.8 V	PCM data output.
8	USB_VBUS	AI	4.0–5.25 V	USB_VBUS	AI	3.0–5.25 V	USB_VBUS	AI	3.0–5.25 V	USB_VBUS	AI	3.0–5.25 V	USB connection detect.
9	USB_DP	AIO	-	USB_DP	AIO	-	USB_DP	AIO	-	USB_DP	AIO	-	USB differential data (+).
10	USB_DM	AIO	-	USB_DM	AIO	-	USB_DM	AIO	-	USB_DM	AIO	-	USB differential data (-).
11	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
12	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
13	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
14	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
15	PWRKEY [9]	DI	-	PWRKEY [10]	DI	-	PWRKEY [10]	DI	-	PWRKEY	DI	-	Turn on/off the module.

[8] When PSM is enabled, the function of PSM_IND pin will be activated after the module is rebooted. When PSM_IND is in high voltage level, the module is in full functionality mode. When it is in low voltage level, the module is in PSM.
[9] For BG95 series, PWRKEY output voltage is 1.5 V because of the voltage drop inside the chipset. Due to platform reasons, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.
[10] For BG96 and EG9x family, PWRKEY output voltage is 0.8 V because of the diode voltage drop inside the chipset.

16	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
17	RESET_N	DI	1.5 V	RESET_N	DI	1.8 V	RESET_N	DI	1.8 V	RESET_N	DI	-	Reset the module.
18	W_DISABLE#	DI	1.8 V	W_DISABLE#	DI	1.8 V	W_DISABLE#	DI	1.8 V	W_DISABLE#*	DI	1.8 V	Airplane mode control.
19	AP_READY	DI	1.8 V	AP_READY	DI	1.8 V	AP_READY	DI	1.8 V	AP_READY*	DI	1.8 V	Application processor ready.
20	STATUS	DO	1.8 V	STATUS	DO	1.8 V	STATUS	DO	1.8 V	STATUS	DO	1.8 V	Indicate the module's operation status.
21	NET_STATUS	DO	1.8 V	NETLIGHT	DO	1.8 V	NETLIGHT	DO	1.8 V	NET_STATUS	DO	1.8 V	Indicate the module's network activity status.
22	DBG_RXD	DI	1.8 V	DBG_RXD	DI	1.8 V	DBG_RXD	DI	1.8 V	DBG_RXD	DI	1.8 V	Debug UART receive.
23	DBG_TXD	DO	1.8 V	DBG_TXD	DO	1.8 V	DBG_TXD	DO	1.8 V	DBG_TXD	DO	1.8 V	Debug UART transmit.
24	ADC0	AI	0.1–1.8 V	ADC0	AI	0.3–1.8 V	ADC0	AI	0.3 V–VBAT_BB	ADC0	AI	0–1.2 V	General-purpose ADC interface.
25	GPIO1 [11]	DIO	1.8 V	RESERVED	-	-	RESERVED	-	-	RESERVED	-	-	1. General-purpose input/output. 2. Reserved.
26	GPIO2	DIO	1.8 V	GPIO26	DIO	1.8 V	SPI_CLK	DO	1.8 V	RESERVED	-	-	1. General-purpose input/output. 2. SPI clock. 3. Reserved.
27	GNSS_TXD	DO	1.8 V	UART3_TXD	DO	1.8 V	SPI_MOSI	DO	1.8 V	GNSS_TXD [12]	DO	1.8 V	1. GNSS UART transmit. 2. UART3 transmit 3. SPI Master out Slave in.
28	GNSS_RXD	DI	1.8 V	UART3_RXD	DI	1.8 V	SPI_MISO	DI	1.8 V	GNSS_RXD [12]	DI	1.8 V	1. GNSS UART receive. 2. UART3 receive. 3. SPI Master in Slave out.
29	VDD_EXT	PO	1.8 V	VDD_EXT	PO	1.8 V	VDD_EXT	PO	1.8 V	VDD_EXT	PO	1.8 V	Provide 1.8 V for external circuit.
30	MAIN_DTR	DI	1.8 V	DTR	DI	1.8 V	DTR	DI	1.8 V	MAIN_DTR	DI	1.8 V	(Main) UART data terminal ready.
31	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
32, 33	VBAT_BB	PI	See ***Table 6***	VBAT_BB	PI	3.3–4.3 V	VBAT_BB	PI	3.3–4.3 V	VBAT_BB	PI	3.3–4.3 V	Power supply for the module's BB part.
34	MAIN_RXD	DI	1.8 V	RXD	DI	1.8 V	RXD	DI	1.8 V	MAIN_RXD	DI	1.8 V	(Main) UART receive.
35	MAIN_TXD	DO	1.8 V	TXD	DO	1.8 V	TXD	DO	1.8 V	MAIN_TXD	DO	1.8 V	(Main) UART transmit.
36	MAIN_CTS	DO	1.8 V	CTS	DO	1.8 V	CTS	DO	1.8 V	MAIN_CTS	DO	1.8 V	DTE clear to send signal from DCE (connect to DTE's CTS).
37	MAIN_RTS	DI	1.8 V	RTS	DI	1.8 V	RTS	DI	1.8 V	MAIN_RTS	DI	1.8 V	DTE request to send signal to DCE (connect to DTE's RTS).
38	MAIN_DCD	DO	1.8 V	DCD	DO	1.8 V	DCD	DO	1.8 V	MAIN_DCD	DO	1.8 V	(Main) UART data carrier detect.

[11] Pin 25 is a general-purpose IO by default. It can be multiplexed into fast shutdown interface with **AT+QCFG="fast/poweroff"**. For details of the command, see ***document [1]***.
[12] For EG91xQ family, GNSS pins are optional. If you need this function, please contact Quectel Technical Support.

39	MAIN_RI	DO	1.8 V	RI	DO	1.8 V	RI	DO	1.8 V	MAIN_RI	DO	1.8 V	(Main) UART ring indication.
40	I2C_SCL	OD	1.8 V only	I2C_SCL	OD	1.8 V only	I2C_SCL	OD	1.8 V	I2C_SCL*	OD	1.8 V	I2C serial clock (for external codec).
41	I2C_SDA	OD	1.8 V only	I2C_SDA	OD	1.8 V only	I2C_SDA	OD	1.8 V	I2C_SDA*	OD	1.8 V	I2C serial data (for external codec).
42	USIM_DET	DI	1.8 V	USIM_ PRESENCE	DI	1.8 V	USIM1_ PRESENCE	DI	1.8 V	USIM1_DET	DI	1.8 V	(U)SIM card hot-plug detect.
43	USIM_VDD	PO	1.8 V	USIM_VDD	PO	1.8/3.0 V	USIM1_VDD	PO	1.8/3.0 V	USIM1_VDD	PO	1.8/3.0 V	(U)SIM1 card power supply.
44	USIM_RST	DO	1.8 V	USIM_RST	DO	1.8/3.0 V	USIM1_RST	DO	1.8/3.0 V	USIM1_RST	DO	1.8/3.0 V	(U)SIM1 card reset.
45	USIM_DATA	DIO	1.8 V	USIM_DATA	DIO	1.8/3.0 V	USIM1_DATA	DIO	1.8/3.0 V	USIM1_DATA	DIO	1.8/3.0 V	(U)SIM1 card data.
46	USIM_CLK	DO	1.8 V	USIM_CLK	DO	1.8/3.0 V	USIM1_CLK	DO	1.8/3.0 V	USIM1_CLK	DO	1.8/3.0 V	(U)SIM1 card clock.
47	USIM_GND	-	-	USIM_GND	-	-	USIM_GND	-	-	GND	-	-	1. Specified ground for (U)SIM card. 2. Ground.
48	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
49	ANT_GNSS	AI	-	ANT_GNSS	AI	-	ANT_GNSS/ ANT_DIV [13]	AI	-	ANT_GNSS [12]	AI	-	1. GNSS antenna interface. 2. Diversity antenna interface.
50	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
51	GNSS_LNA_ EN [14]	DO	-	RESERVED	-	-	NC	-	-	GNSS_PPS [12]	DO	1.8 V	1. External LNA enable control. 2. Reserved. 3. Not connected. 4. GNSS pulse per second output
52, 53	VBAT_RF	PI	See ***Table 6***	VBAT_RF	PI	3.3–4.3 V	VBAT_RF	PI	3.3–4.3 V	VBAT_RF	PI	3.3–4.3 V	Power supply for the module's RF part.
54, 55	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
56	ANT_WIFI [15]	AI	-	RESERVED	-	-	ANT_DIV/ RESERVED [16]	AI/-	-	RESERVED	-	-	1. Wi-Fi antenna interface. 2. Reserved. 3. Diversity antenna interface.
57	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
58, 59	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
60	ANT_MAIN	AIO	-	ANT_MAIN	AIO	-	ANT_MAIN	AIO	-	ANT_MAIN	AIO	-	Main antenna interface.
61, 62	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.

[13] For EG91 series, pin 49 is defined as ANT_GNSS on EG91-AUX/-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as ANT_DIV on EG91-E. For EG95 series, pin 49 is defined as ANT_GNSS on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as ANT_DIV on EG95-E.
[14] Only BG95-M4/-MF support GNSS_LNA_EN (pin 51).
[15] Only BG95-MF supports ANT_WIFI (pin 56).
[16] For EG91 series, pin 56 is defined as ANT_DIV on EG91-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as RESERVED on EG91-AUX/-E. Rx-diversity antenna is not supported on EG91-AUX. For EG95 series, pin 56 is defined as ANT_DIV on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as RESERVED on EG95-E.

63	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
64	GPIO3 [17]	DIO	1.8 V	GPIO64	DIO	1.8 V	NC	-	-	RESERVED	-	-	1. General-purpose input/output. 2. Not connected. 3. Reserved.
65	GPIO4 [17]	DIO	1.8 V	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. General-purpose input/output. 2. Reserved. 3. Not connected.
66	GPIO5	DIO	1.8 V	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. General-purpose input/output. 2. Reserved. 3. Not connected.
67–74	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
75	USB_BOOT	DI	1.8 V	USB_BOOT	DI	1.8 V	USB_BOOT	DI	1.8 V	USB_BOOT	DI	1.8 V	1. BG9x & EG9x: Make the module enter forced download mode. 2. EG91xQ: Make the module enter download mode. Only in download mode, the module supports firmware upgrade over USB 2.0 interface.
76	RESERVED	-	-	RESERVED	-	-	GRFC9/NC [18]	DO/-	1.8 V	GRFC1	DO	1.8 V	1. Reserved. 2. Generic RF controller. 3. Not connected.
77	RESERVED	-	-	RESERVED	-	-	GRFC10/NC [18]	DO/-	1.8 V	GRFC2	DO	1.8 V	1. Reserved. 2. Generic RF controller. 3. Not connected.
78	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_SPI_CLK*	DI	1.8 V	1. Reserved. 2. Not connected. 3. Camera SPI clock.
79–82	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
83	GRFC1 [19]	DO	1.8 V	RESERVED	-	-	USIM2_PRESENCE	DI	1.8 V	RESERVED	-	-	1. Generic RF controller. 2. Reserved. 3. (U)SIM2 card hot-plug detect.
84	GRFC2 [19]	DO	1.8 V	RESERVED	-	-	USIM2_CLK	DO	1.8/3.0 V	USIM2_CLK [20]	DO	1.8 V	1. Generic RF controller. 2. Reserved. 3. (U)SIM2 card clock.
85	GPIO6	DIO	1.8 V	RESERVED	-	-	USIM2_RST	DO	1.8/3.0 V	USIM2_RST [20]	DO	1.8 V	1. General purpose input/output. 2. Reserved. 3. (U)SIM2 card reset.
86	GPIO7	DIO	1.8 V	RESERVED	-	-	USIM2_DATA	DIO	1.8/3.0 V	USIM2_DATA	DIO	1.8 V	1. General purpose input/output.

[17] BG95-MF does not support GPIO3 and GPIO4 interfaces (pins 64 and 65).
[18] For EG91 series, pins 76 and 77 are respectively defined as GRFC9 and GRFC10 on EG91-AUX/-JP, while they are defined as NC on EG91-E/-EX/-NA/-NAX/-NAXD/-VX. For EG95 series, pins 76 and 77 are respectively defined as GRFC9 and GRFC10 on EG95-AUX/-JP, while they are defined as NC on EG95-E/-EX/-NA/-NAX/-NAXD.
[19] BG95-M4/-M9 do not support GRFC interfaces (pins 83 and 84).
[20] For EG91xQ family, USIM2 and Camera SPI* cannot be used at the same time.

										[20]			2. Reserved. 3. (U)SIM2 card data.
87	GPIO8	DIO	1.8 V	RESERVED	-	-	USIM2_VDD	PO	1.8/3.0 V	USIM2_VDD [20]	PO	1.8 V	1. General purpose input/output. 2. Reserved. 3. (U)SIM2 card power supply.
88	GPIO9	DIO	1.8 V	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. General purpose input/output. 2. Reserved. 3. Not connected.
89–91	GND	-	-	GND	-	-	GND	-	-	GND	-	-	Ground.
92	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
93	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_VDDIO*	PO	1.8 V	1. Reserved. 2. Not connected. 3. Camera digital power supply.
94	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_VDD*	PO	2.8 V	1. Reserved. 2. Not connected. 3. Camera analog power supply.
95	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_MCLK*	DO	1.8 V	1. Reserved. 2. Not connected. 3. Master clock of the camera.
96	PON_TRIG	DI	1.8 V	RESERVED	-	-	NC	-	-	PSM_INT*	DI	1.8 V	1. Wake up the module from power saving mode. 2. Reserved. 3. Not connected.
97	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_SPI_DATA0*	DI	1.8 V	1. Reserved. 2. Not connected. 3. Camera SPI data bit 0.
98	RESERVED	-	-	RESERVED	-	-	NC	-	-	CAM_SPI_DATA1*	DI	1.8 V	1. Reserved. 2. Not connected. 3. Camera SPI data bit 1.
99	RESERVED	-	-	RESERVED	-	-	NC	-	-	RESERVED	-	-	1. Reserved. 2. Not connected.
100–102	GND	-	-	RESERVED	-	-	GND	-	-	GND	-	-	1. Ground. 2. Reserved.
103–106	-	-	-	-	-	-	GND	-	-	RESERVED	-	-	1. Ground. 2. Reserved.
107–108	-	-	-	-	-	-	-	-	-	RESERVED	-	-	Reserved.
109	-	-	-	-	-	-	-	-	-	GNSS_DBG_TXD [12]	DO	1.8 V	GNSS debug UART transmit.
110	-	-	-	-	-	-	-	-	-	GNSS_DBG_RXD [12]	DI	1.8 V	GNSS debug UART receive.
111	-	-	-	-	-	-	-	-	-	RESERVED	-	-	Reserved.

112	-	-	-	-	-	-	-	-	-	GNSS_RST [12]	DI	1.8 V	GNSS chip reset.
113-114	-	-	-	-	-	-	-	-	-	RESERVED	-	-	Reserved.
115	-	-	-	-	-	-	-	-	-	CAM_PWDN*	DO	1.8 V	Camera power down.
116	-	-	-	-	-	-	-	-	-	RESERVED	-	-	Reserved.
117	-	-	-	-	-	-	-	-	-	GNSS_PWR_EN [12]	DI	1.8 V	GNSS power enabled.
118	-	-	-	-	-	-	-	-	-	GNSS_VBCKP [12]	PI	1.9–3.6 V	Power supply for GNSS RTC.
119-126	-	-	-	-	-	-	-	-	-	RESERVED	-	-	Reserved.

NOTE

1. Pins 103–106 in **purple** are additional pins on EG9x and EG91xQ families that are not available on BG9x family. Pins 107–126 in **purple** are additional pins on EG91xQ family that are not available on BG9x and EG9x families.
2. Pins in **blue** are pins with different functions or voltage domain on BG9x, EG9x and EG91xQ families, but the module footprint is compatible.
3. Pins in **black** are compatible pins on BG9x, EG9x and EG91xQ families with the same functionality.

4 Hardware Interface Design

4.1. Power Supply

Table 9: Pin Difference of VBAT_BB & VBAT_RF

Pin Name	Pin No.	DC Characteristics			
		BG95 Series	BG96	EG9x Family	EG91xQ Family
VBAT_BB	32, 33	**BG95-M1/-M2** [21]**:** Vmax = 4.8 V Vmin = 2.6 V Vnom = 3.3 V **BG95-M3/-M5/ -M6/-MF/-M8:** Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V
VBAT_RF	52, 53	**BG95-M4/-M9:** Vmax = 4.2 V Vmin = 3.2 V Vnom = 3.8 V **VBAT_BB:** Imax = 0.6 A **VBAT_RF:** Imax = 2.7 A	**VBAT_BB:** Imax = 0.5 A **VBAT_RF:** Imax = 2.7 A	**VBAT_BB:** Imax = 0.8 A **VBAT_RF:** Imax = 1.8 A	**VBAT_BB:** Imax = 0.5 A **VBAT_RF:** Imax = 1.5 A

[21] For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should exceed 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full functionality mode, the minimum power supply voltage should exceed 2.8 V.

NOTE

1. BG9x family are LPWA modules, which require low quiescent and leakage current. For more information about sufficient current for BG9x family, see ***documents [2]*** and ***[3]***.
2. The power supply of EG9x and EG91xQ families should be able to provide sufficient current of at least 2.0 A.
3. See the corresponding reference design documents of the modules for more details about power supply design.

- **BG95 Series**

Use two TVS components with low leakage current and suitable reverse standoff voltage to ensure power source stability. It is recommended to place them as close to VBAT pins as possible.

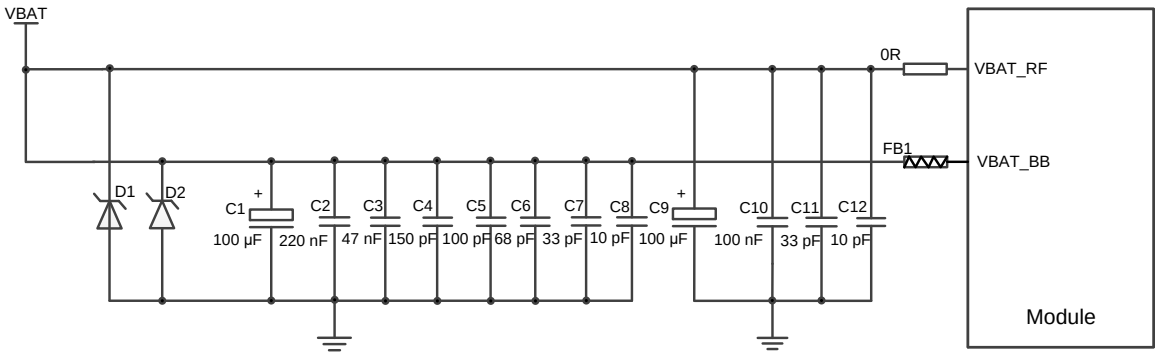


Figure 3: Power Supply in Star Structure (BG95 Series)

- **BG96 & EG91xQ Family**

Use a TVS with low reverse standoff voltage V_{RWM} (4.7 V), low clamping voltage V_C and high reverse peak pulse current I_{PP} to ensure power source stability. The power supply in star structure is presented in the figure below.

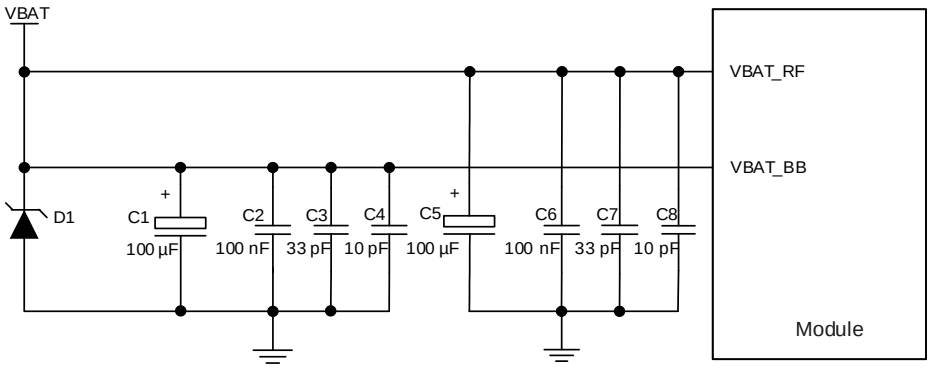
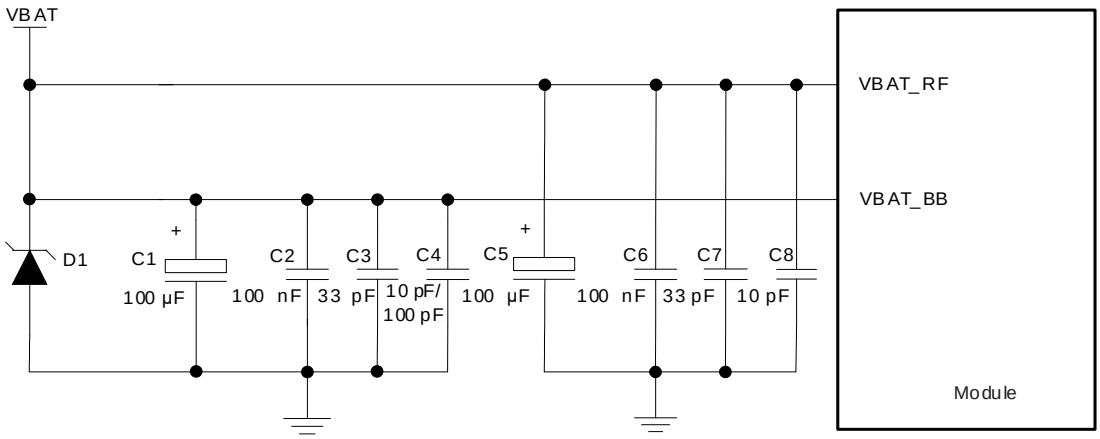


Figure 4: Power Supply in Star Structure (BG96 & EG91xQ Family)

- **EG9x Family**

To avoid the damage caused by electric surge and ESD, it is suggested that a TVS with recommended low reverse standoff voltage V_{RWM} (4.5 V), low clamping voltage V_C and high reverse peak pulse current I_{PP} should be used. The following figure shows power supply in star structure.



NOTE:
For EG9x-AUX/-E/-EX/-JP, the capacitance of C4 is 10 pF.
For EG9x-NA/-NAX/-NAXD and EG91-VX, the capacitance of C4 is 100 pF.

Figure 5: Power Supply in Star Structure (EG9x Family)

4.2. Turn On/Off

The turn-on/off method is the same for BG9x, EG9x and EG91xQ families. The modules can be turned on or turned off after pressing PWRKEY for a certain time.

4.2.1. Turn On

Turn-on circuits of the modules are presented in the figures below.

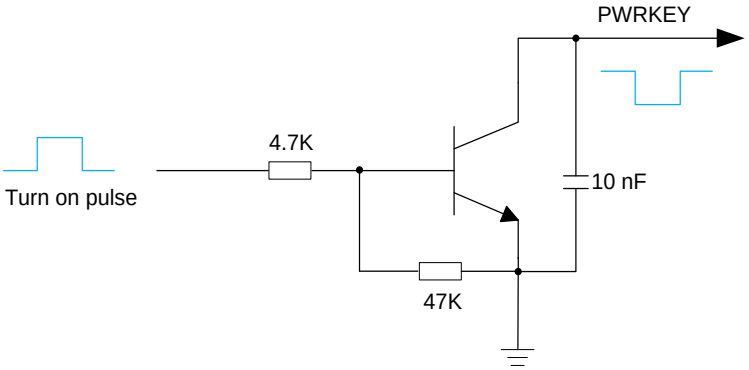


Figure 6: Turn On Modules with a Driving Circuit

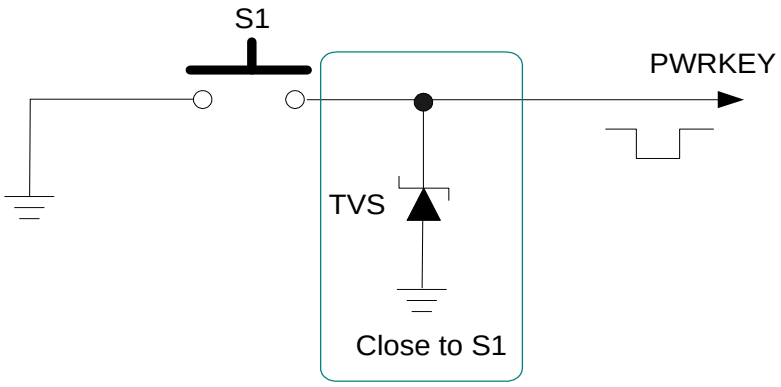


Figure 7: Turn On Modules with a Button

The power-up timing of the modules is illustrated in the figure below.

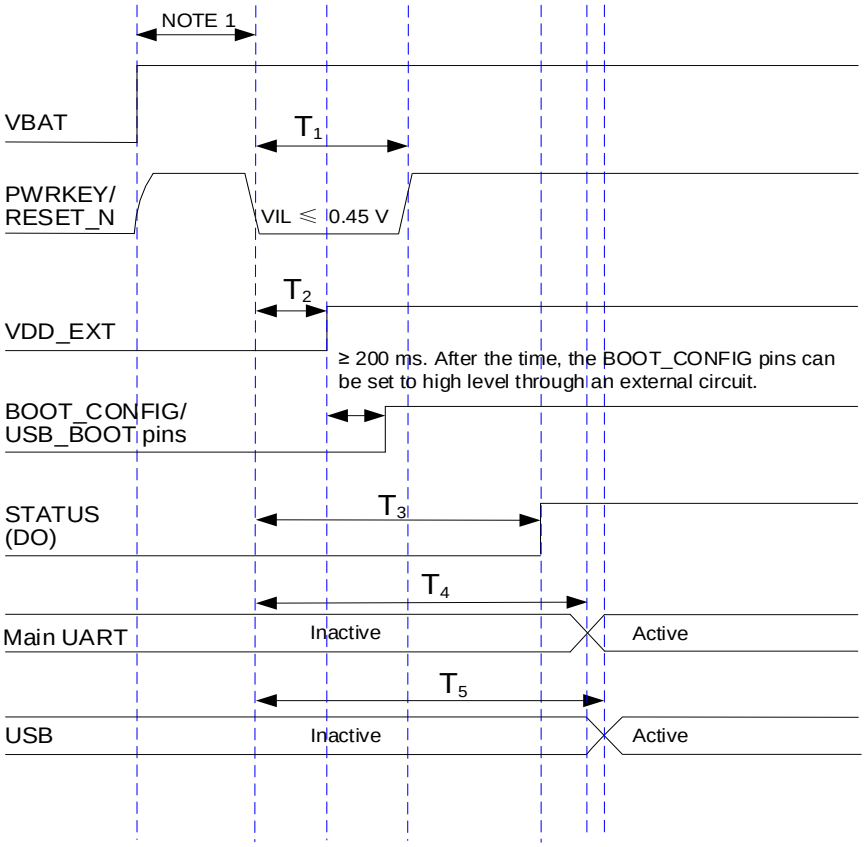


Figure 8: Power-up Timing (BG95 Series)

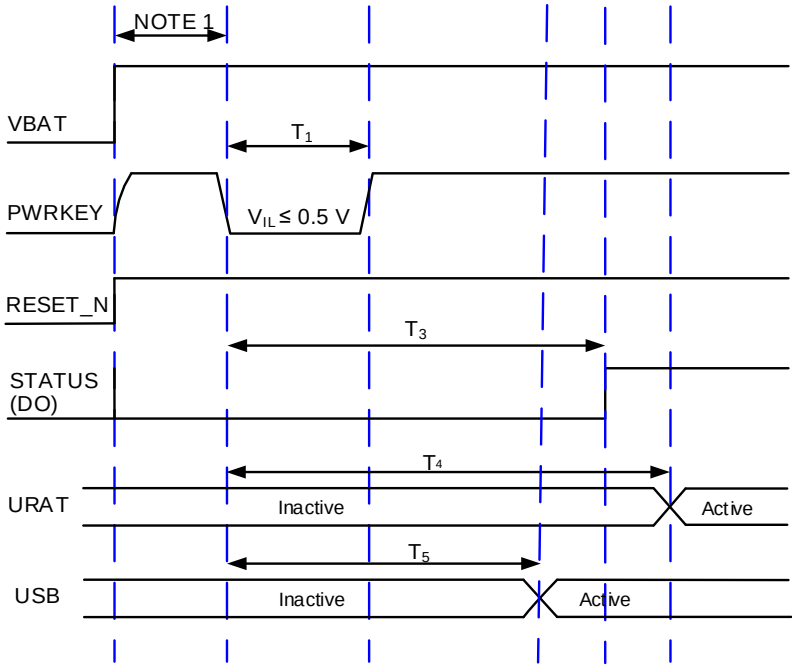


Figure 9: Power-up Timing (BG96)

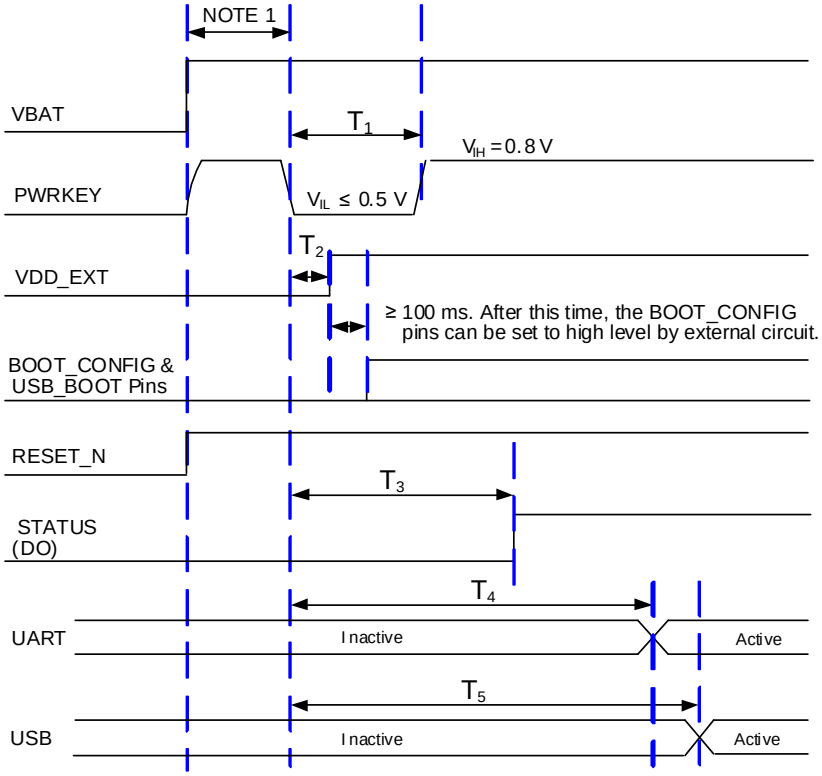


Figure 10: Power-up Timing (EG9x Family)

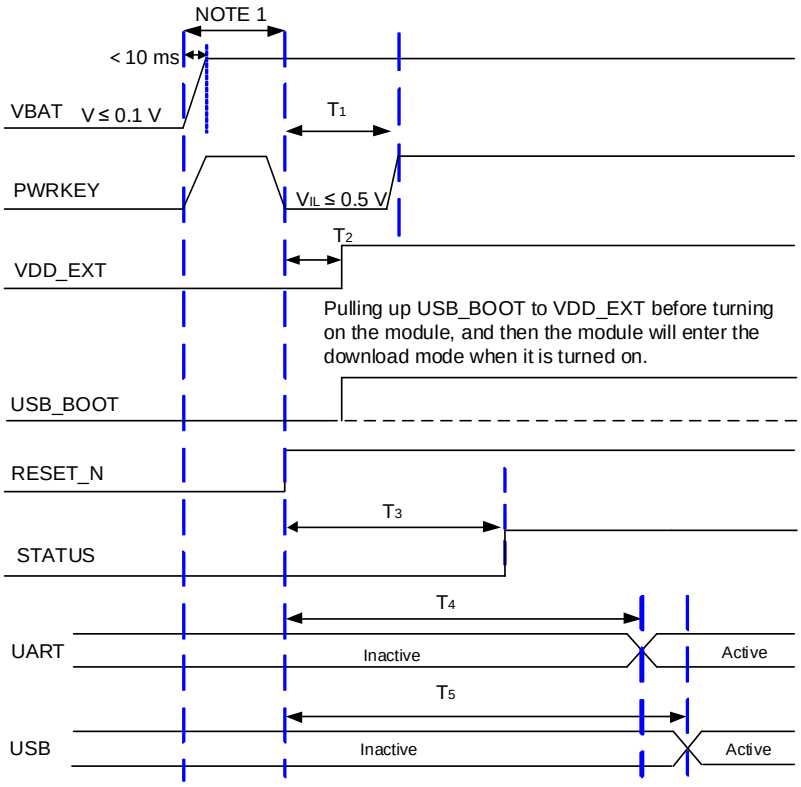


Figure 11: Power-up Timing (EG91xQ Family)

Table 10: Power-up Timing

Module	T_1	T_2	T_3	T_4	T_5
BG95 series	500–1000 ms	About 30 ms	≥ 2.1 s	≥ 2.5 s	≥ 2.55 s
BG96	≥ 500 ms	-	≥ 4.8 s	≥ 4.9 s	≥ 4.2 s
EG9x family	≥ 500 ms	About 100 ms	≥ 10 s	≥ 12 s	≥ 13 s
EG91xQ family	≥ 500 ms	About 40 ms	≥ 2 s	≥ 10 s	≥ 10 s

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY, and maintain an interval of at least 30 ms.
2. BOOT_CONFIG pins on BG95 series and EG9x family cannot be pulled up before startup.
3. PWRKEY can be pulled down directly to GND with a recommended 10 kΩ (for EG9x family) or 4.7 kΩ (for EG91xQ family) resistor if the modules need to be powered on automatically and shutdown is not needed.
4. For BG95 series, PWRKEY output voltage is 1.5 V because of the voltage drop inside the chipset.

Due to platform reasons, the reset function is integrated into PWRKEY on the chipset. Therefore, never pull down PWRKEY to GND permanently.

5. For BG96 and EG9x family, PWRKEY output voltage is 0.8 V because of the diode voltage drop inside the chipset.

4.2.2. Turn Off

4.2.2.1. Turn Off with PWRKEY

The following is power-down timing for BG9x, EG9x and EG91xQ families.

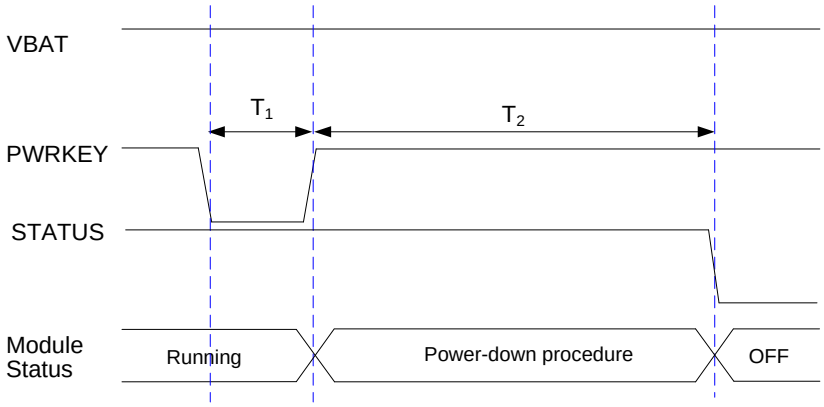


Figure 12: Power-down Timing

Table 11: Power-down Timing with PWRKEY

Module	T_1	T_2
BG95 series	650–1000 ms	≥ 1.3 s
BG96	≥ 650 ms	≥ 2 s
EG9x family	≥ 650 ms	≥ 30 s
EG91xQ family	≥ 650 ms	≥ 1.35 s

4.2.2.2. Turn Off with AT Command

The modules can also be safely turned off with **AT+QPOWD**, which is similar to turning off the modules via PWRKEY pin. See ***documents [4]***, ***[5]***, ***[6]*** and ***[7]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply while the module is working normally. The power supply can be cut off only after the module is shut down with PWRKEY or AT command.
2. For EG9x and EG91xQ families, when turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

4.3. Reset

BG9x and EG9x families can be reset by driving RESET_N low for a certain time or directly via a button.

For EG91xQ family, the reset function is activated by using both the PWRKEY and RESET_N pins. The module can be reset by pulling down PWRKEY when RESET_N is at low level.

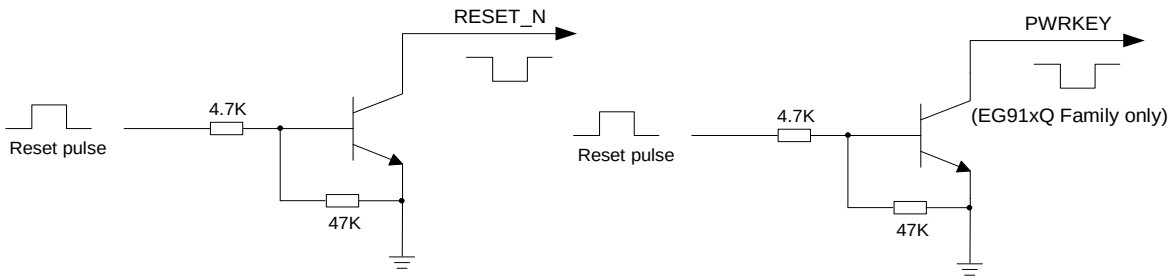


Figure 13: Reference Design of RESET_N with a Driving Circuit

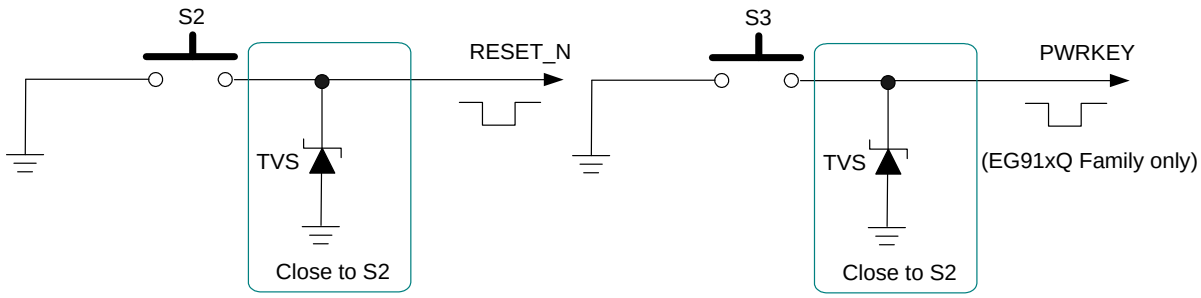


Figure 14: Reference Circuit of RESET_N by Using Button

The reset timing for BG9x and EG9x families is illustrated in the following figure.

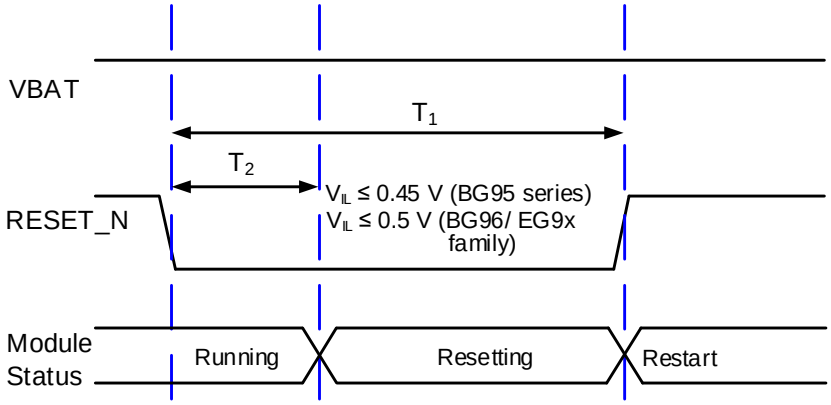


Figure 15: Reset Timing (BG9x & EG9x Families)

Table 12: Reset Timing

Module	T_1	T_2
BG95 series	≤ 3.8 s	≥ 2 s
BG96	≤ 460 ms	≥ 150 ms
EG9x family	≤ 460 ms	≥ 150 ms

The reset timing for EG91xQ family is illustrated in the following figure.

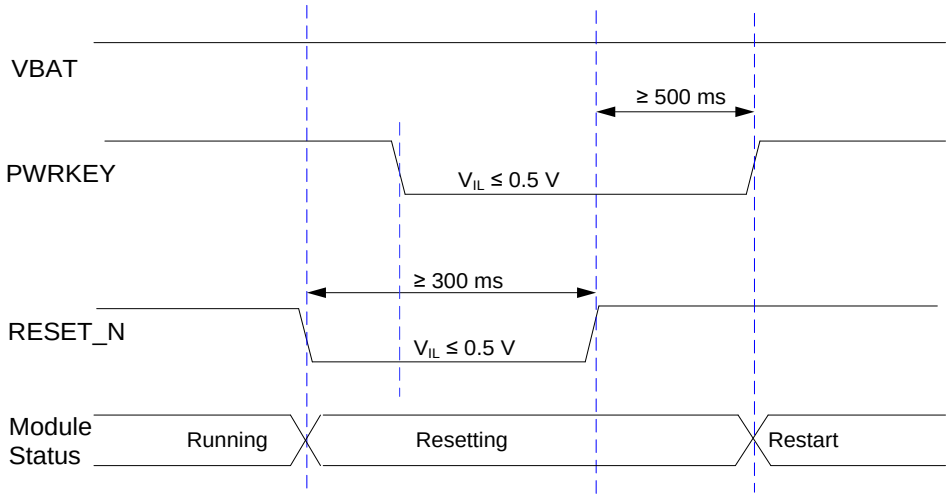


Figure 16: Reset Timing (EG91xQ Family)

NOTE

1. Use RESET_N function only if turn-off with **AT+QPOWD** and PWRKEY pin fails.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.
3. For BG95 series:
   - Due to platform reasons, the reset function is integrated into PWRKEY on the chipset, and RESET_N is directly connected to PWRKEY inside the module.
   - RESET_N should not be pulled down to GND permanently.

4.4. (U)SIM Interface(s)

- BG9x family: one (U)SIM interface
- EG9x & EG91xQ families: two (U)SIM interfaces.

Table 13: Pin Difference of (U)SIM Interfaces

Pin No.	BG95 Series	BG96	EG9x Family	EG91xQ Family	Comment
42	USIM_DET	USIM_ PRESENCE	USIM1_ PRESENCE	USIM1_DET	1.8 V power domain.
43	USIM_VDD	USIM_VDD	USIM1_VDD	USIM1_VDD	**BG95 series:** Only 1.8 V (U)SIM card is supported.
44	USIM_RST	USIM_RST	USIM1_RST	USIM1_RST	
45	USIM_DATA	USIM_DATA	USIM1_DATA	USIM1_DATA	**BG96 & EG9x & EG91xQ families:** Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
46	USIM_CLK	USIM_CLK	USIM1_CLK	USIM1_CLK	
47	USIM_GND	USIM_GND	USIM_GND	GND	-
83	-	-	USIM2_ PRESENCE	-	1.8 V power domain.
84	-	-	USIM2_CLK	USIM2_CLK	**EG9x family:** 1.8 V or 3.0 V (U)SIM2 card is supported.
85	-	-	USIM2_RST	USIM2_RST	
86	-	-	USIM2_DATA	USIM2_DATA	**EG91xQ family:** USIM2 interface only supports 1.8 V power domain.
87	-	-	USIM2_VDD	USIM2_VDD	

NOTE

1. **BG9x family:**
   - (U)SIM2 interface is not supported.
2. **EG91xQ family:**
   - When USIM1 and USIM2 are used at the same time, the power domain of USIM interfaces should be 1.8 V. Otherwise, USIM2 interface will be damaged.
   - USIM2 and Camera SPI* cannot be used at the same time.

4.5. USB Interface

BG9x, EG9x, EG915Q-NA and EG916Q-GL provide one integrated Universal Serial Bus (USB) interface, which complies with USB 2.0 specification and only supports USB slave mode.

Table 14: Data Rate and Function of USB Interface

Module	Data Rate	Function
BG9x family	● High-speed (480 Mbps) ● Full-speed (12 Mbps) ● Low-speed (1.5 Mbps) (Only supported on **BG95 series**)	● AT command communication ● Data transmission [22] ● Software debugging ● Firmware upgrade ● GNSS NMEA sentence output
EG9x family	● High-speed (480 Mbps) ● Full-speed (12 Mbps)	● AT command communication ● Data transmission ● Software debugging ● Firmware upgrade ● GNSS NMEA sentence output ● Voice over USB
EG91xQ family		● AT command communication ● Data transmission ● Software debugging ● Firmware upgrade ● GNSS NMEA sentence output (**All-in-one** mode only) ● Partial log output

[22] It is not recommended to use USB for data communication, as this will increase the power consumption.

NOTE

The GNSS function for BG96, EG9x and EG91xQ families is optional.

Table 15: Pin Difference of USB_VBUS

Pin Name	Pin No.	I/O	DC Characteristics	
			BG95 Series	BG96 & EG9x & EG91xQ Families
USB_VBUS	8	AI	Vmax= 5.25 V Vmin = 4.0 V Vnom = 5.0 V	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V

For BG9x and EG9x families, it is recommended to reserve the USB interface for firmware upgrade.

For EG91xQ family, test points of USB 2.0 interface must be reserved, which can be used for firmware upgrade and software debugging.

Following figures illustrate the reference design of USB interface.

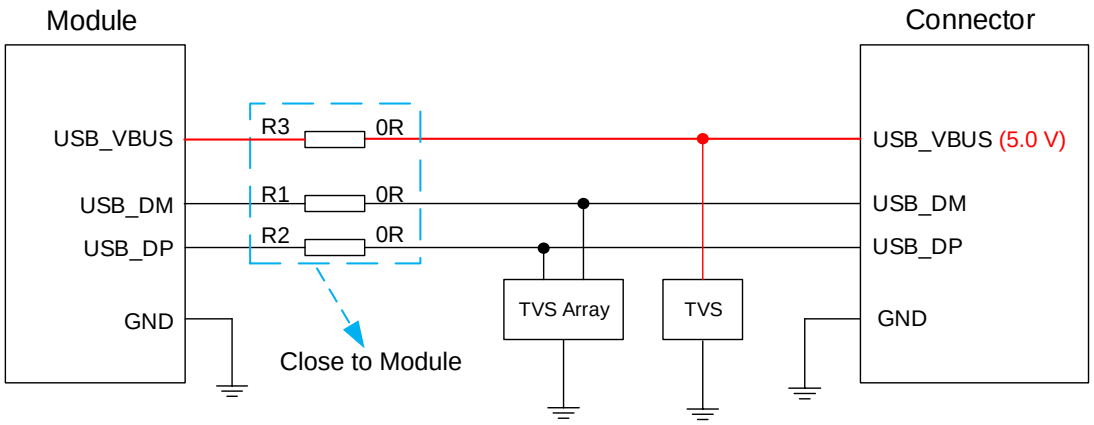


Figure 17: Reference Design of USB Interface (BG95 Series)

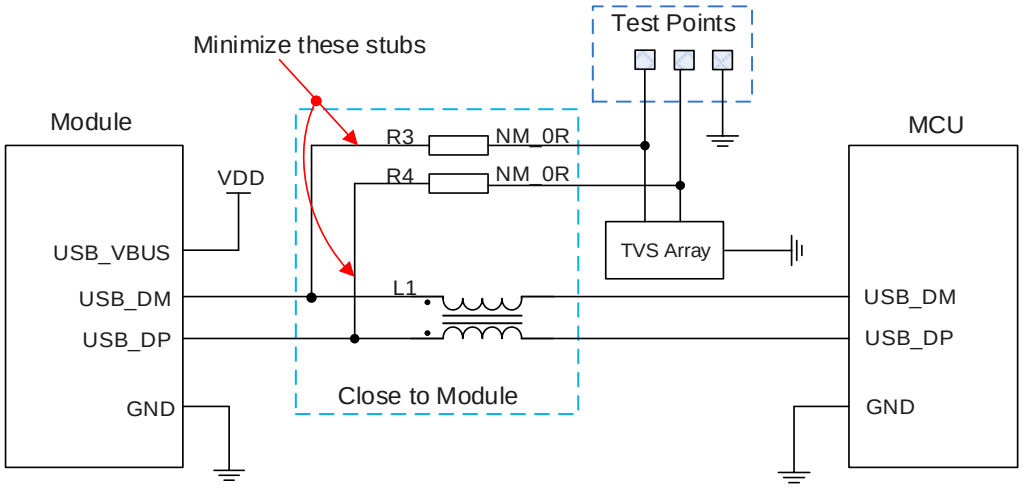


Figure 18: Reference Design of USB Interface (BG96 & EG9x & EG91xQ Families)

4.6. PCM and I2C Interfaces* [23]

BG9x, EG9x and EG91xQ families provide one PCM interface and one I2C interface.

The following table illustrates the modes supported by PCM and I2C interfaces.

Table 16: Modes Supported by PCM and I2C Interfaces

Modules	PCM Interface	I2C Interface
BG9x family	Master mode only	Master mode only
EG9x family	Slave and master modes [24]	Master mode only
EG91xQ family	TBD	TBD

The following figure illustrates the reference design of PCM and I2C application with audio codec for BG9x, EG9x and EG91xQ families.

[23] The PCM and I2C interfaces of EG91xQ family are still under development.
[24] In short frame synchronization, EG9x family modules work as both master and slave device. In long frame synchronization, EG9x family modules work as master device only.

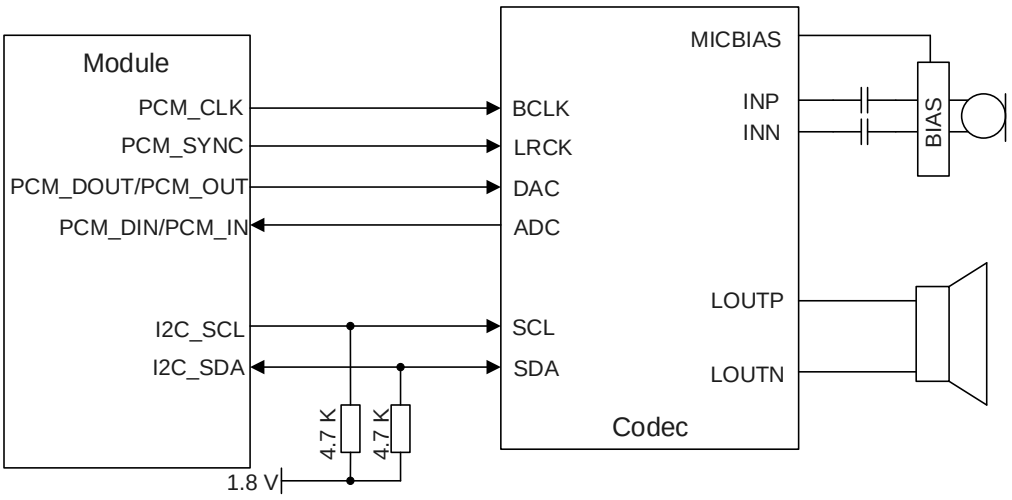


Figure 19: PCM and I2C Application with Audio Codec

4.7. UART Interfaces

UART interfaces supported by BG9x, EG9x and EG91xQ families are listed below.

Table 17: Supported UART Interfaces

Modules	UART Interfaces
BG9x family	1. Main UART 2. Debug UART 3. GNSS UART
EG9x family	1. Main UART 2. Debug UART
EG91xQ family	1. Main UART 2. Debug UART 3. GNSS UART 4. GNSS debug UART

Table 18: Pin Difference of UART Interfaces

UART	Pin No.	BG95 Series	BG96	EG9x Family	EG91xQ Family
Main UART	30	MAIN_DTR	DTR	DTR	MAIN_DTR
	34	MAIN_RXD	RXD	RXD	MAIN_RXD

	35	MAIN_TXD	TXD	TXD	MAIN_TXD
	36	MAIN_CTS	CTS	CTS	MAIN_CTS
	37	MAIN_RTS	RTS	RTS	MAIN_RTS
	38	MAIN_DCD	DCD	DCD	MAIN_DCD
	39	MAIN_RI	RI	RI	MAIN_RI
Debug UART	22	DBG_RXD	DBG_RXD	DBG_RXD	DBG_RXD
	23	DBG_TXD	DBG_TXD	DBG_TXD	DBG_TXD
GNSS UART	28	GNSS_RXD	UART3_RXD	-	GNSS_RXD
	27	GNSS_TXD	UART3_TXD	-	GNSS_TXD
GNSS debug UART	110	-	-	-	GNSS_DBG_RXD
	109	-	-	-	GNSS_DBG_TXD

NOTE

For EG91xQ family, GNSS UART and GNSS debug UART interfaces are optional. If you need these functions, please contact Quectel Technical Support.

4.8. ADC Interfaces

BG9x & EG91xQ families: two ADC interfaces (ADC0 & ADC1).

EG9x family: one ADC interface (ADC0).

Table 19: Pin Difference of ADC Interfaces

Pin Name	Pin No.	I/O	DC Characteristics			
			BG95 Series	BG96	EG9x Family	EG91xQ Family
ADC0	24	AI	0.1–1.8 V	0.3–1.8 V	0.3 V–VBAT_BB	0–1.2 V
ADC1	2	AI			-	

4.9. Antenna Interfaces

ANT_MAIN of BG9x, EG9x and EG91xQ families are compatible with each other, whereas BG95 series' GNSS and Wi-Fi antenna interfaces, BG96 and EG91xQ family's GNSS antenna interface, EG9x family's Rx-diversity and GNSS antenna interfaces are not compatible.

Table 20: Pin Definition of Antenna Interfaces

Pin No.	I/O	BG95 Series	BG96	EG9x Family	EG91xQ Family	Comment
60	AIO	ANT_MAIN	ANT_MAIN	ANT_MAIN	ANT_MAIN	50 Ω impedance.
49	AI	ANT_GNSS	ANT_GNSS	ANT_GNSS/ ANT_DIV [25]	ANT_GNSS	
56	AI	ANT_WIFI [26]	-	ANT_DIV/ RESERVED [27]	-	

It is recommended to reserve a Π-type matching circuit for better RF performance, and the Π-type matching components (R1, C1, C2, and R2, C3, C4) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

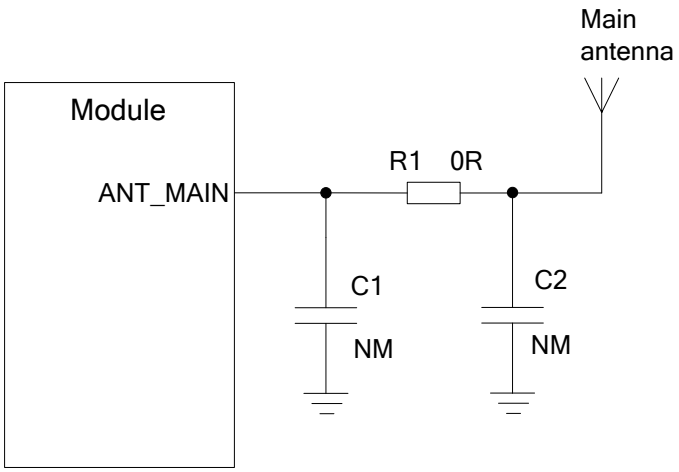


Figure 20: Main Antenna Interfaces (BG9x & EG91xQ Families)

[25] For EG91 series, pin 49 is defined as ANT_GNSS on EG91-AUX/-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as ANT_DIV on EG91-E. For EG95 series, pin 49 is defined as ANT_GNSS on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as ANT_DIV on EG95-E.
[26] Only BG95-MF supports ANT_WIFI (pin 56).
[27] For EG91 series, pin 56 is defined as ANT_DIV on EG91-EX/-JP/-NA/-NAX/-NAXD/-VX, while it is defined as RESERVED on EG91-AUX/-E. Rx-diversity antenna is not supported on EG91-AUX. For EG95 series, pin 56 is defined as ANT_DIV on EG95-AUX/-EX/-JP/-NA/-NAX/-NAXD, while it is defined as RESERVED on EG95-E.

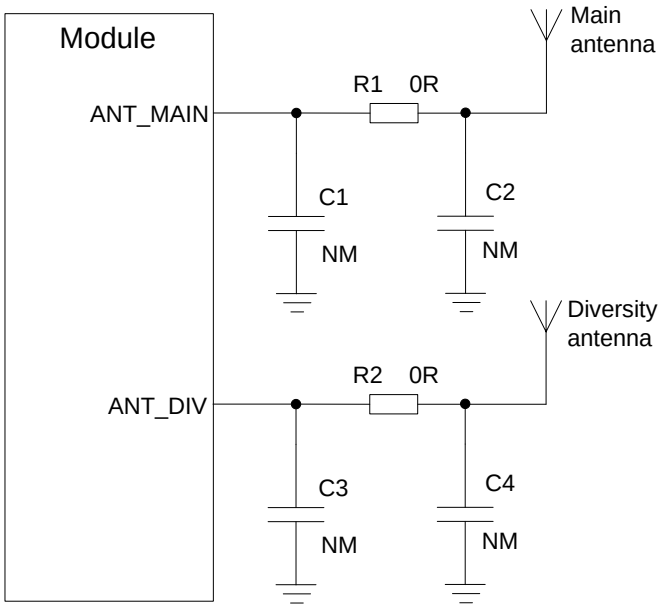


Figure 21: Main and Rx-diversity Antenna Interfaces (EG9x Family)

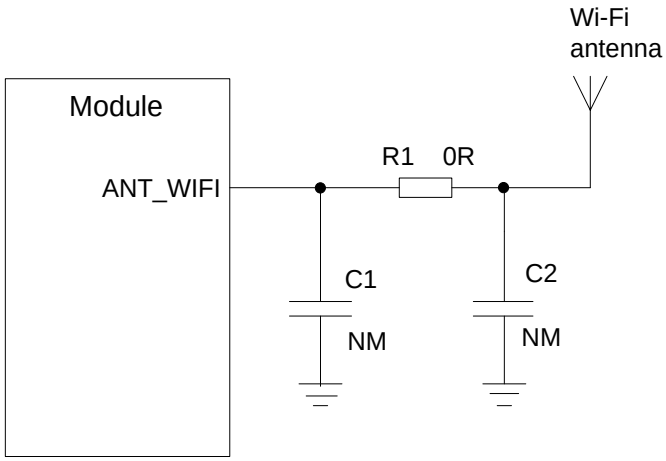


Figure 22: Wi-Fi Antenna Interface (BG95 Series)

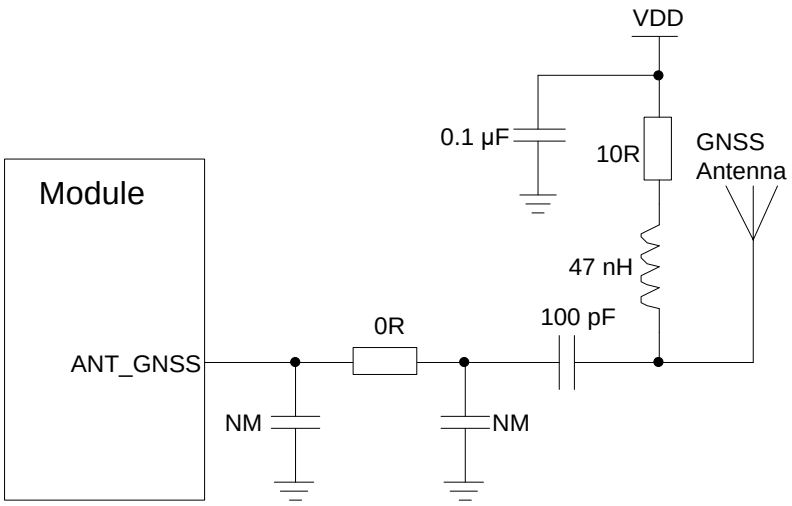


Figure 23: GNSS Antenna Interface

NOTE

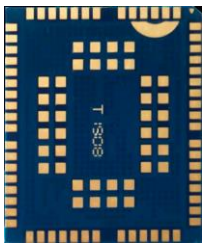
1. For the GNSS antenna of BG9x, EG9x and EG91xQ families, if the module is designed with a passive antenna, then the VDD circuit is not needed.
2. ANT_GNSS of EG91xQ family is optional.

5 Recommended Footprint

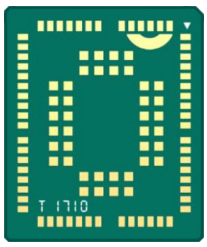
This chapter primarily describes the recommended footprint and stencil design for BG9x, EG9x and EG91xQ families. All dimensions are measured in mm, and the dimensional tolerances are ±0.2 mm.

5.1. Recommended Compatible Footprint

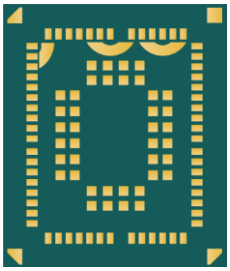
The following figure shows the bottom views of the modules.



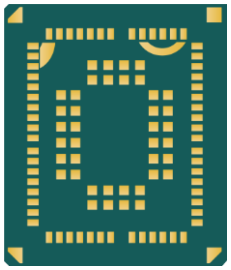
BG95 Series



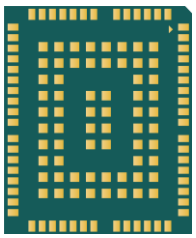
BG96



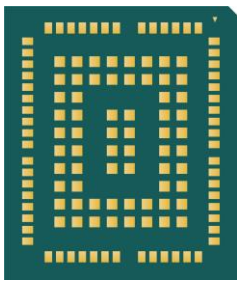
EG9x-AUX/-EX/-JP/-NA/-NAX/-NAXD, EG91-VX



EG9x-E



EG915Q-NA



EG916Q-GL

Figure 24: Bottom Views

NOTE

Images above are for illustrative purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

The following figure shows the recommended compatible footprint of BG9x, EG9x and EG91xQ families.

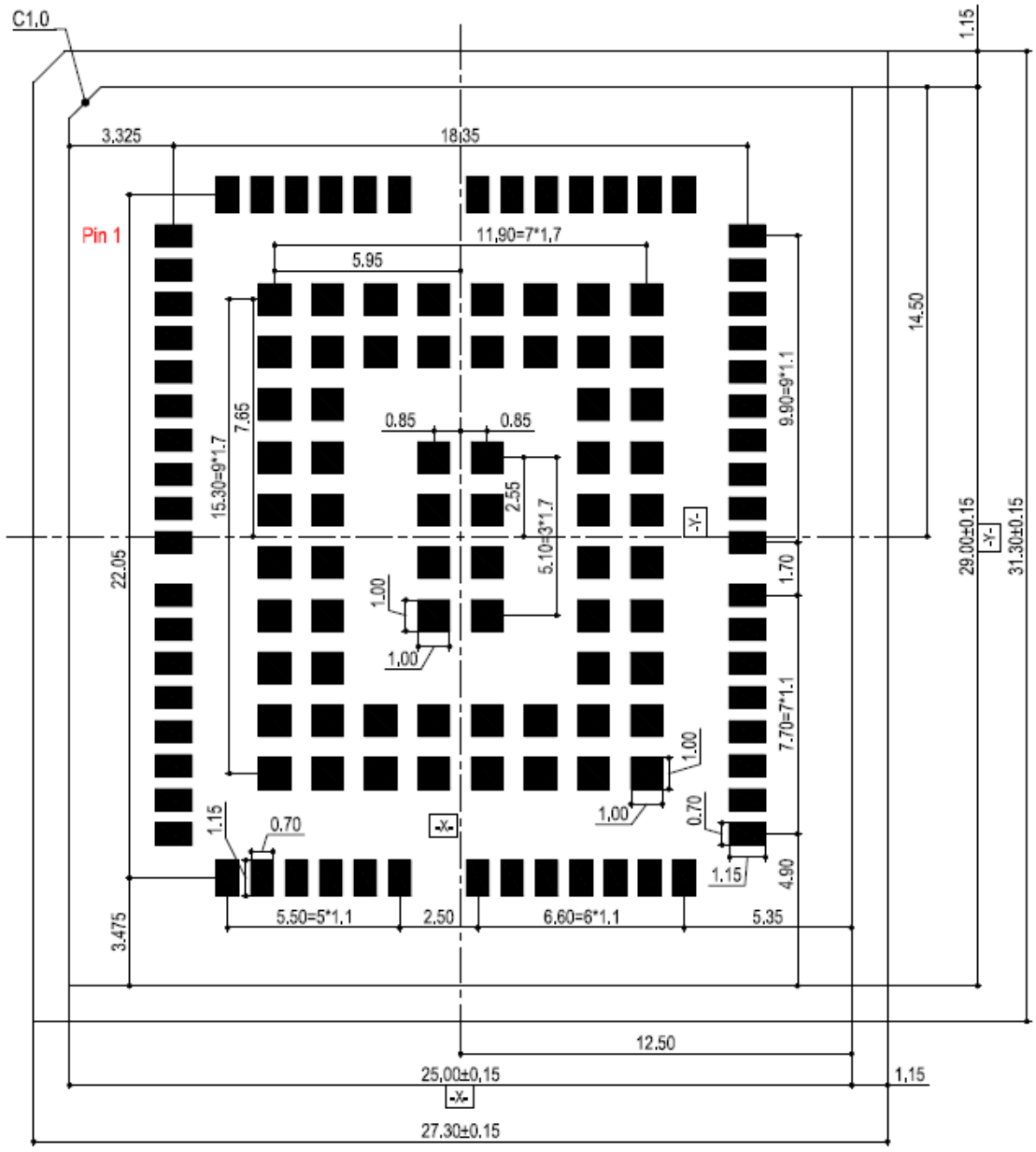


Figure 25: Recommended Compatible Footprint

NOTE

1. The package warpage level of the module refers to the *JEITA ED-7306* standard.
2. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

5.2. Installation Sketch Map

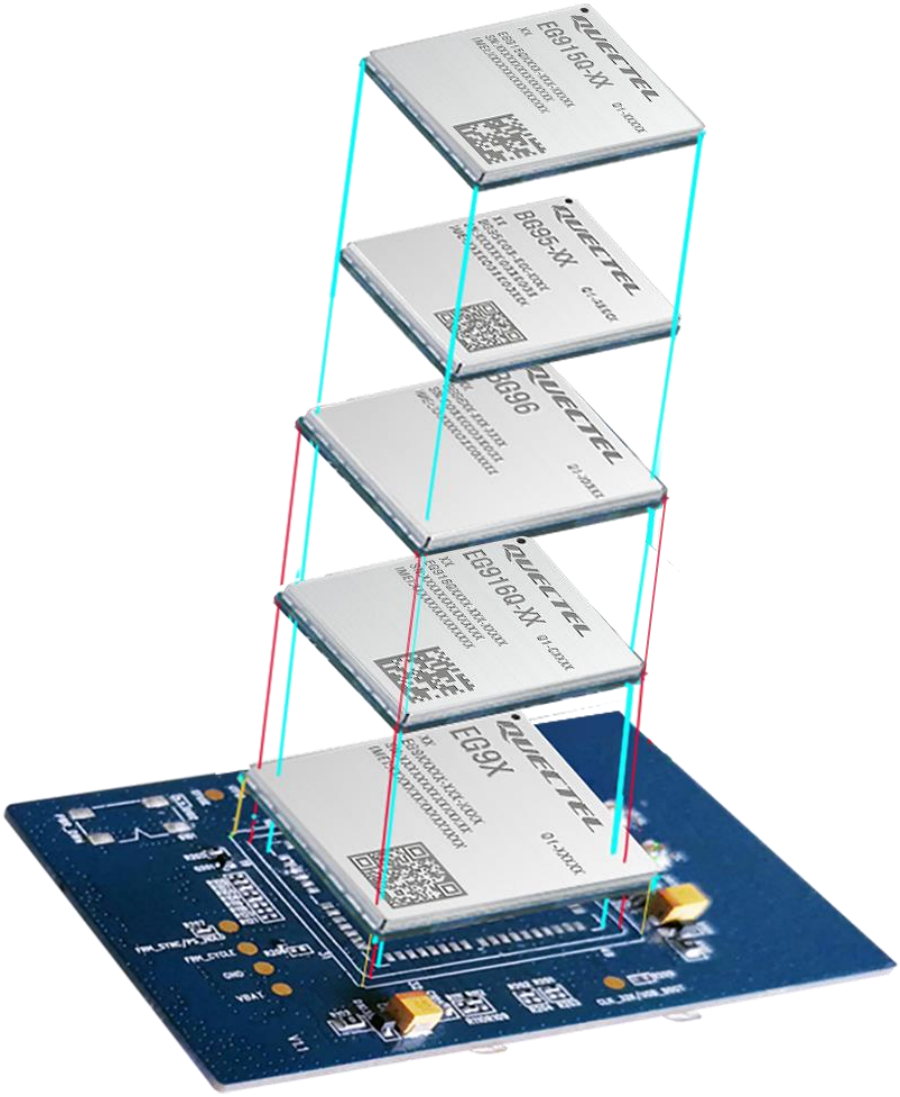


Figure 26: Installation Sketch Map

6 Appendix References

Table 21: Related Documents

Document Name
[1] Quectel_BG95&BG77&BG600L_Series_QCFG_AT_Commands_Manual
[2] Quectel_BG95_Series_Hardware_Design
[3] Quectel_BG96_Hardware_Design
[4] Quectel_BG95&BG77&BG600L_Series_AT_Commands_Manual
[5] Quectel_BG96_AT_Commands_Manual
[6] Quectel_EC2x&EG2x-G(L)&EG9x&EM05_Series_AT_Commands_Manual
[7] Quectel_EG800Q&EG91xQ_Series_AT_Commands_Manual

Table 22: Terms and Abbreviations

Abbreviation	Description
bps	bits per second
CS	Coding Scheme
CTS	Clear To Send
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DFOTA	Delta Firmware Upgrade Over The Air
DRX	Discontinuous Reception
DTR	Data Terminal Ready
EGPRS	Enhanced General Packet Radio Service

FDD	Frequency Division Duplex
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
IoT	Internet of Things
LGA	Land Grid Array
LPWA	Low-Power Wide-Area (Network)
LTE	Long Term Evolution
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
PCM	Pulse Code Modulation
PF	Paging Frame
PSM	Power Saving Mode
RF	Radio Frequency
Rx	Receive
SMS	Short Message Service
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage

VoLTE	Voice (voice calls) over LTE
WCDMA	Wideband Code Division Multiple Access